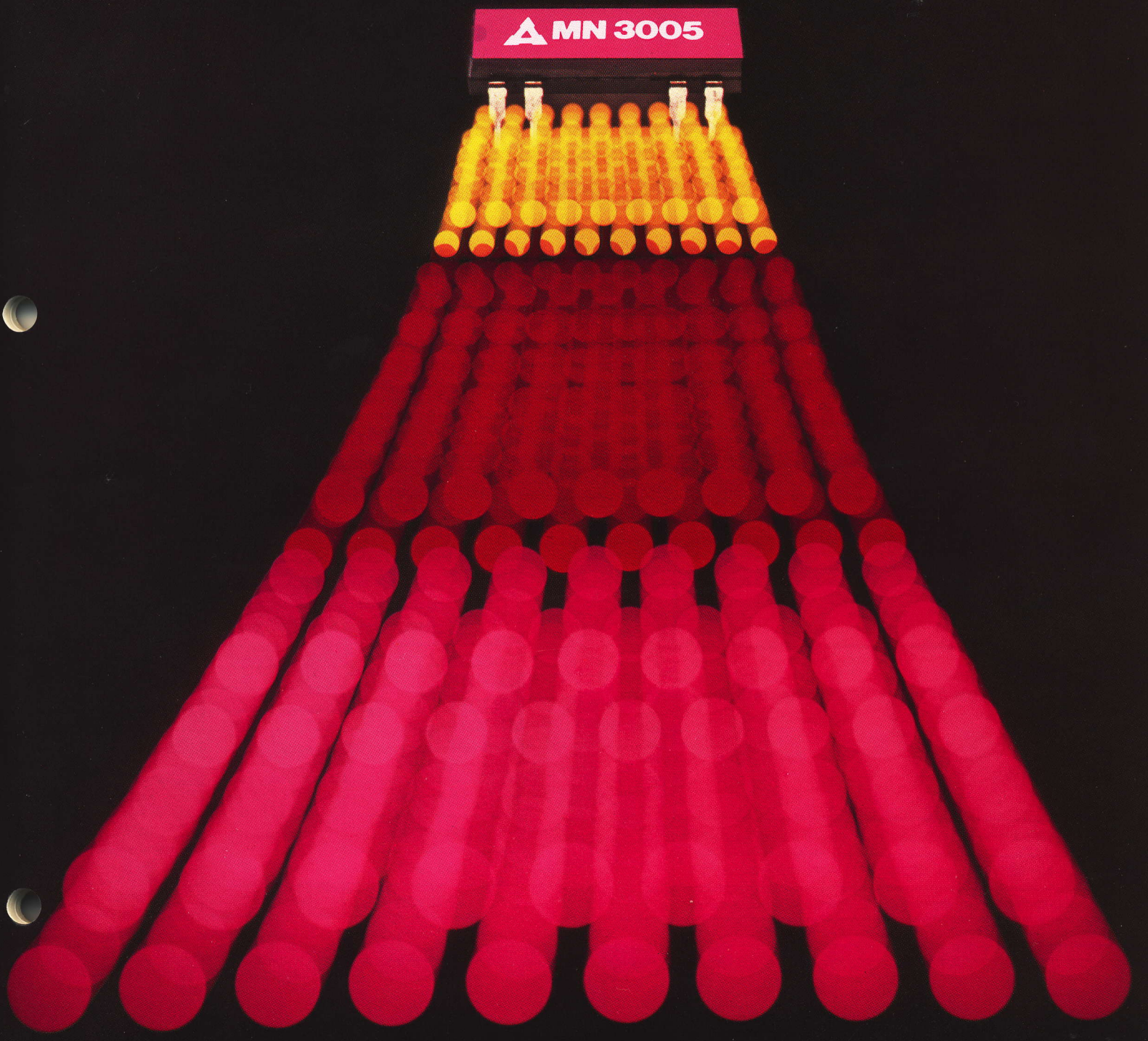
Panasonic®

BBD Bucket Brigade Devices



BBD SERIES
Bucket Brigade Devices

Panasonic holds a leadership position in the area of BBD's for audio signal delays. Since the first BBD (type MN3001) was developed, various new types have been introduced to meet the expanding market requirement. Now the product range has expanded to twelve types, ranging from 64-stage to the longest 4096-stage BBD.

This edition of our "BBD Series" catalog contains detailed information on the twelve types of products in this series already in production. If further information is required for your BBD application, please feel free to contact our sales offices, representatives or distributors. We always wish to offer you better service to satisfy your quality and performance requirements.

CONTENTS

INTRODUCTION 1
TYPICAL APPLICATIONS 1
CLOCK FREQUENCY and SIGNAL DELAY TIME 1
SELECTION GUIDE by STAGES 1
BBD QUICK REFERENCE TABLE 2
SPECIFICATIONS and CHARACTERISTICS
MN3001, MN3002 3
MN3003 9
MN3004 13
MN3005 18
MN3006 23
MM3007 28
MN3008 32
MN3009 36
MN3010 40
MN3011 44
MN3012 50
MN3101 56

The device specifications are subject to change without prior notice. While every precaution has been taken in the preparation of this data sheet, the publisher assumes no responsibility for patent liability with respect to the use of the information contained herein.

INTRODUCTION

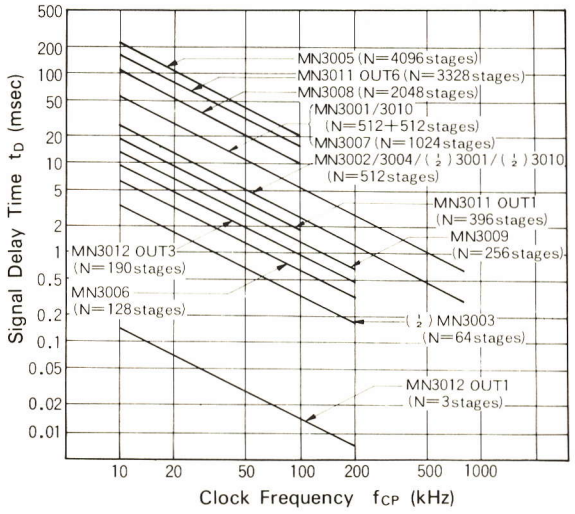
The Bucket Brigade Device is a P-channel silicon gate MOS LSI consists of a number of bucket brigade stages fabricated on a single chip. Each stage consists of a capacitor that stores the electrical charge and a tetrode transistor for switching purposes. Electrical charges corresponding to analog signals are transferred from one stage to another by a two phase clock drive. Thus the electric signals flow unidirectionally from the input to the output with a time delay which can be controlled by the clock frequency.

The Bucket Brigade Device has found a variety of applications in audio equipment as a useful variable or fixed delay line. The device can obtain chorus and tremolo effects in electronic musical instruments as well as reverberation effects in audio equipment, which completely replaces conventional mechanical systems. The device can also be used to restore the correct pitch of tape recordings played back faster or slower than the correct speed to accommodate the listener's rate of comprehension. In addition to these applications, the BBD facilitates the production of equipment incorporating new concepts with high marketability.

TYPICAL APPLICATIONS

- **Variable speech control of playback and voice control of tape recorders.**
- **Reverberation effect of echo microphones and stereo equipment.**
- **Tremolo, vibrato and/or chorus effects in electronic musical instruments.**
- **Variable or fixed delay of analog signals.**

CLOCK FREQUENCY AND SIGNAL DELAY TIME



SELECTION GUIDE by STAGES

Stage		Type No.	Noise	Application
64	Dual Type	**MN3003**	Low Noise Types	Reverberation Effect (Signal Delay under 10 msec.) Vibrato Effect *1 Chorus Effect *2 Phasor/Flanger Effect *3
128		**MN3006**		
3, 5, 190	Triple Type	**MN3012**		
256	Single Type	**MN3009**		
512	Single Type	**MN3004**		Echo Effect (Signal Delay over 10 msec.) Double Voicing Effect *4
		MN3002	Standard Types	
	Dual Type	**MN3001**		
		MN3010	Low Noise Types	
1024	Single Type	**MN3007**		
2048		**MN3008**		Reverberation Effect (Signal Delay over 100 msec.)
4096		**MN3005**		Reverberation Effect (Signal Delay over 100 msec.)
3328	Multi-Type	**MN3011**		Reverberation Effect (Six different delay outputs)

*1 Vibrato Effect: Several Hz moduration effect of the clock frequency for BBD.
*2 Chorus Effect: Mixing effect of the original signal and the attenuated delayed signal.
*3 Phasor/Flanger Effect: Effect of either the sum or difference of the original signal and the delayed signal.
*4 Double Voicing Effect: Mixing effect of the original signal and the delayed signal.

BBD QUICK REFERENCE TABLE

Item		Symbol	MN3001	MN3002	MN3003	MN3004	MN3005	MN3006	MN3007	MN3008	MN3009	MN3010	MN3011	MN3012	Unit
	Number of BBD	N	Dual-512	512	Dual-64	512	4096	128	1024	2048	256	Dual-512	3328 6-Tap	190, 3, 5 3-Tap	Stage
Circuit Construction	Clock Generator		External		Built-in	External								Built-in	
	Output Terminal				Pair								6 Different Taps	3 Different Taps	
Operating Conditions	Drain Supply Voltage	V_{DD}	−15		−9	−15	−15	−15	−15	−15	−15	−15	−15	−15	V
	Gate Supply Voltage	V_{GG}	−14		−8	−14	−14	−14	−14	−14	−14	−14	−14	−	V
	Back-Gate Bias Voltage	V_{BB}	+5		Not Needed										V
	Clock Voltage "H" Level	VCPH	0		0	0	0 ~ −1	0 ~ −1	0 ~ −1	0 ~ − 1	0 ~ −1	0 ~ −1	0 ~ −1.3	−0 ~ −0.4	V
	Clock Voltage "L" Level	VCPL	−15		−9	−15	−15	−15	−15	−15	−15	−15	−15	−15	V
	Input DC Bias	VBias	−3.3~−4.9		−2.5~−6	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−5~−10	−5 ~ −10	−	−3~−12	V
Electrical Characteristics	Input Signal Frequency	fi	12				10	12			14	12	10	12	kHz (max.)
	Input Signal Swing	Vi	1.8		0.8	1.8	1.2	1.8	1.5	1.5	1.7	1.8	1.0	1.2	Vrms (max.)
	Insertion Loss	Li	8.5		3.5	1.5	0	0	0	0	0	0	0	0	dB (typ.)
	Total Harmonic Distortion	THD	0.4		0.5	0.4	1	0.2	0.5	0.5	0.3	0.4	0.4	0.4	% (typ.)
	Noise Voltage	Vno	250 (typ.)		140	210	400	200	300	300	150	210	0.4	0.14	μVrms (max.)
	Signal to Noise Ratio	S/N	70		75	85	75	90	80	78	88	85	76	OUT1 = 90 OUT2 = 97 OUT3 = 98	dB (typ.)
	Signal Delay Time	tD	51.2	25.6	6.4	25.6	204.8	6.4	51.2	102.4	12.8	51.2	t_{D1} = 198 331 597 863 1395 1664	0.475 ~ 9.5 0.0125 ~ 0.25 0.0075 ~ 0.15	msec (max.)
Package (Molded Package)			14-Pin DIP				Larger 8-Pin DIP	8-Pin DIP		Larger 8-Pin DIP	8-Pin DIP	14-Pin DIP	12-Pin DIP	14-Pin DIP	

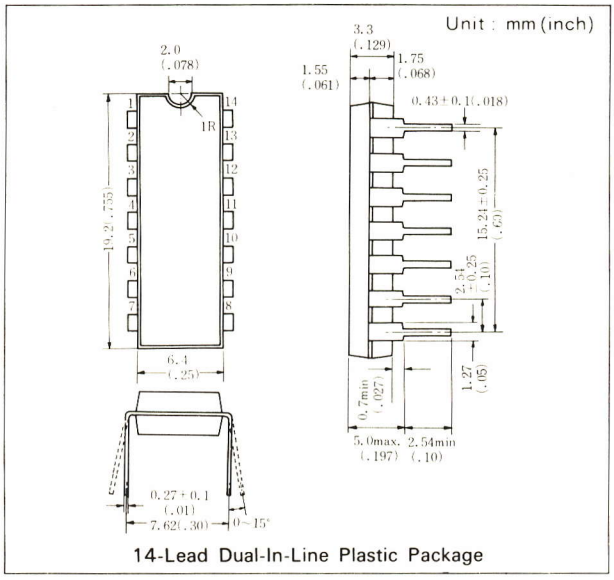
MN3001/MN3002

DUAL 512-STAGE BBD (MN3001), 512-STAGE BBD (3002)

General Description

The MN3001 is a dual 512-stage BBD which contains two identical BBD's on a single chip with independent input, output and clock terminals as well as common power supply terminals. Each 512-stage BBD provides a signal delay of up to 25.6msec. The two identical BBD's integrated on the same chip offer uniform Characteristics and space saving advantage when they are used in parallel or series connection.

The MN3002 is a single 512-stage BBD that provides a signal delay of up to 25.6msec.



14-Lead Dual-In-Line Plastic Package

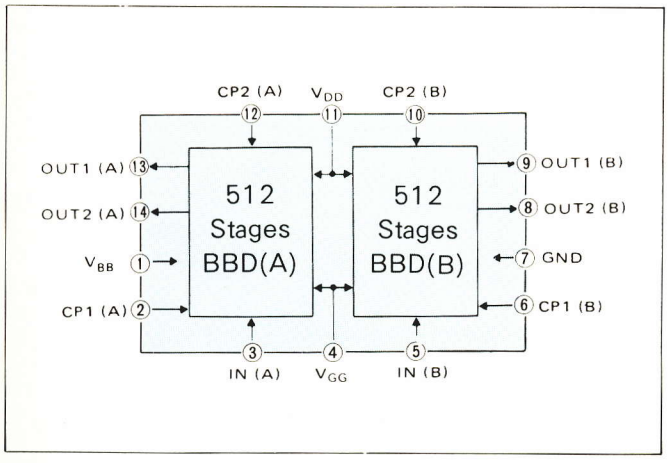
Features:

- Valiable delay line in audio frequency range:
  0.32~25.6msec. (512-stage)
  0.64~51.2msec. (512×2-stage)
- Clock component cancellation capability.
- Wide dynamic range: S/N 70dB typ.
- Wide frequency response: $f_i \leq 0.3 \times f_{CP}$
- Low distortion: THD=0.4% typ.
- Wide clock frequency range: 10~800kHz
- Low noise: Vno=0.25mVrms typ.
- Small DC level shift under wide clock frequency change: 40mV typ. (f_{CP}=10~300kHz)
- P-channel silicon gate, tetrode MOS transistors configuration.
- 14-lead dual-in-line plastic package.

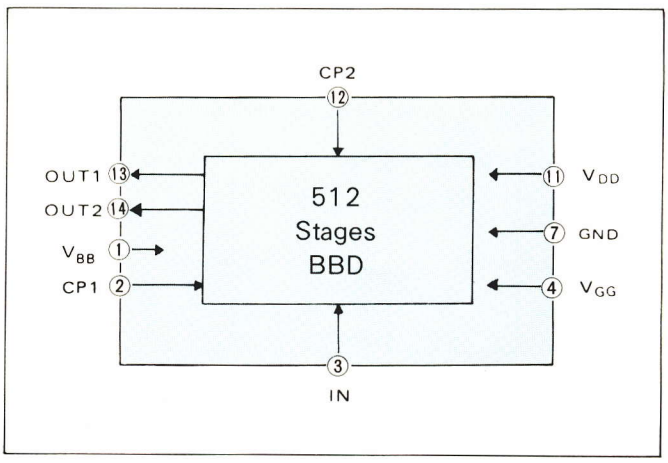
Applications:

- Tremolo, vibrato and/or chorus effects in electronic musical instruments.
- Reverberation effect of stereo equipment.
- Variable or fixed delay of analog signals.

Block Diagram (MN3001)



Block Diagram (MN3002)



Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−20~+0.3	V
Back-gate Bias Voltage	V_{BB}	−0.3~+10	V
Power Dissipation	P_D	50	mW
Operating Temperature	Topr	−20~+60	°C
Storage Temperature	Tstg	−55~+125	°C

Operating Conditions (Ta=25°C)

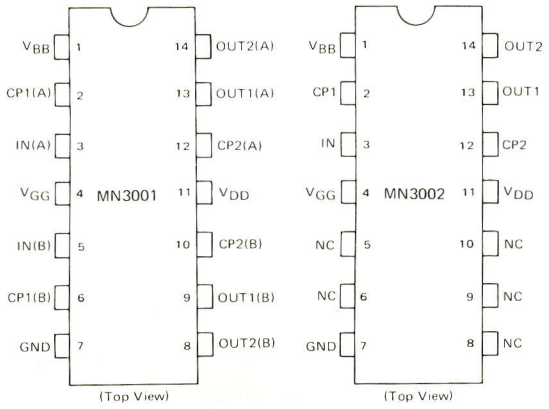
Item	Symbol	Condition	Typical Value	Unit
Drain Supply Voltage	V_{DD}		−15	V
Gate Supply Voltage	V_{GG}		−14	V
Back-gate Bias Voltage	V_{BB}	V_{CPH}=0~−1V	+5 *1	V
Clock Voltage "H" Level	V_{CPH}	V_{BB}=+4~+6V	0 *1	V
Clock Voltage "L" Level	V_{CPL}		−15	V
Clock Frequency	f_{CP}		40	kHz
Clock Pulse Width *3	tcpw		0.5 T max. *2	
Clock Rise Time *3	tcpr		0.05T max.	
Clock Fall Time *3	tcpf		0.05T max.	
Clock Input Capacitance	C_{CP}		250	pF
Input DC Bias Voltage	V_{Bias}		−3.3~−4.9	V

Electrical Characteristics (Ta=25°C, V_{DD}=V_{CPL}=−15V, V_{GG}=−14V, V_{GG}=+5V, R_L=100KΩ)

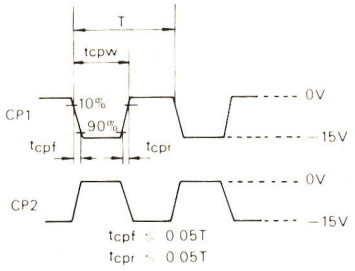
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		0.32		25.6	msec
Input Signal Frequency	f_i	f_{CP}=40kHz, V_i= 2 Vrms, 3dB down (0 dB at f_i=1kHz)	0		0.3f_{CP}	kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i=1kHz, THD ≦ 2.5%			1.8	Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i=1kHz, V_i=2Vrms		8.5	11	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.4	2.5	%
Noise Voltage	Vno	f_{CP}=80kHz, Weighted by "A" curve		0.25		mVrms
Signal to Noise Ratio	S/N			70		dB

*1 The device can be used at V_{BB}=0V when V_{CPH} is set at −3V.
*2 T=1/fcp (Clock Period)
*3 Clock Pulse Waveforms

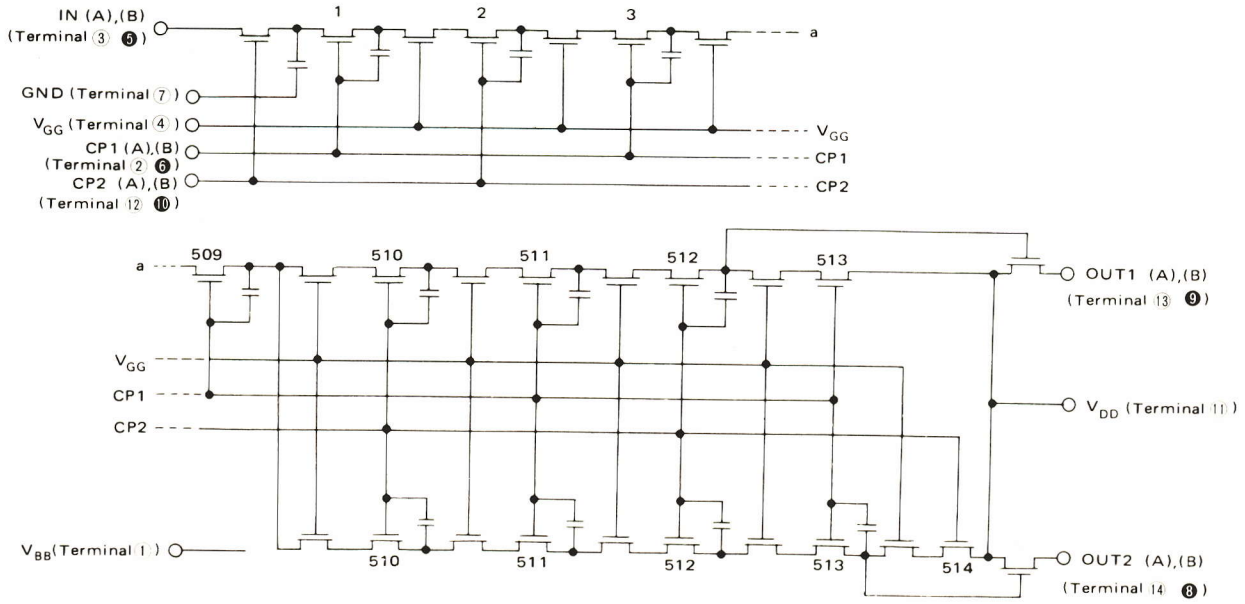
Terminal Assignments



Clock Pulse Waveforms

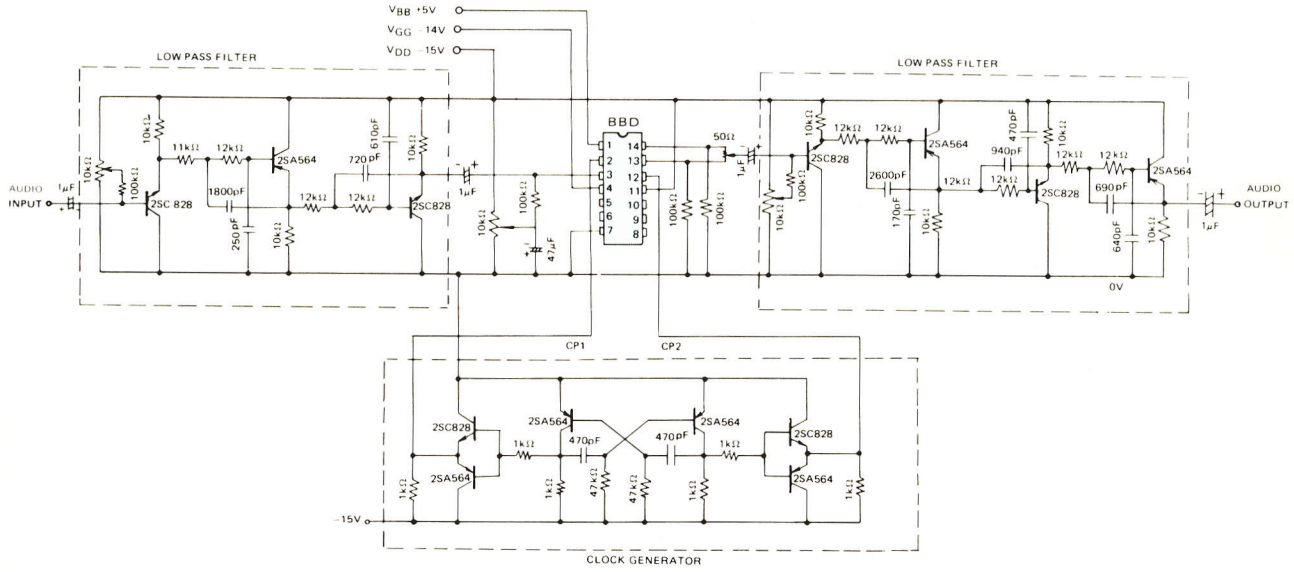


CIRCUIT DIAGRAM



Note: Terminals CP1❻, CP2❿, IN❺, OUT1❾, OUT2❽ are usable for the MN3001, and no-connection for the MN3002.

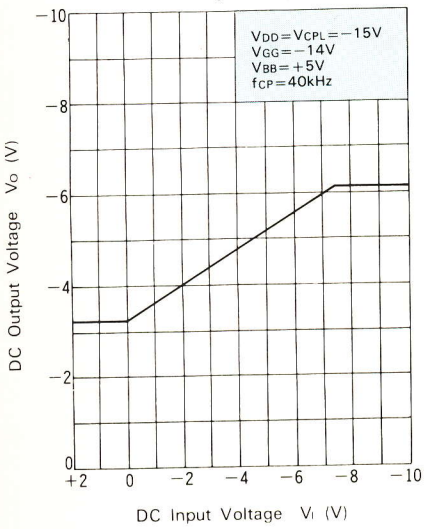
TEST CIRCUIT EXAMPLE



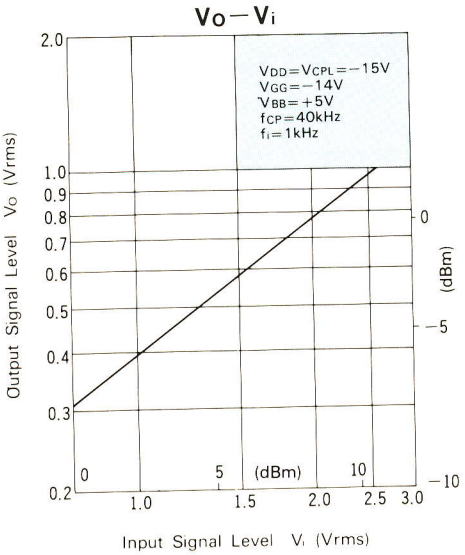
Insertion Loss Measuring Circuit.

Typical Electrical Characteristic Curves

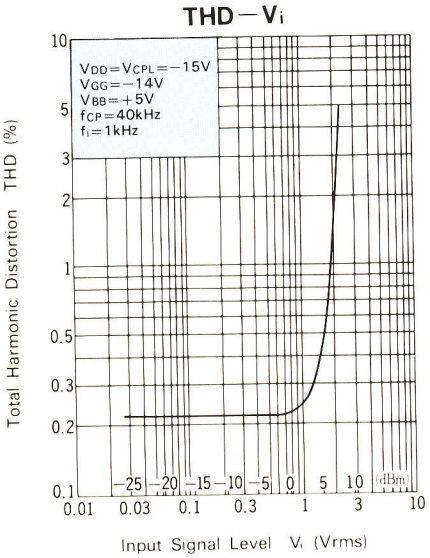
$V_O - V_I$



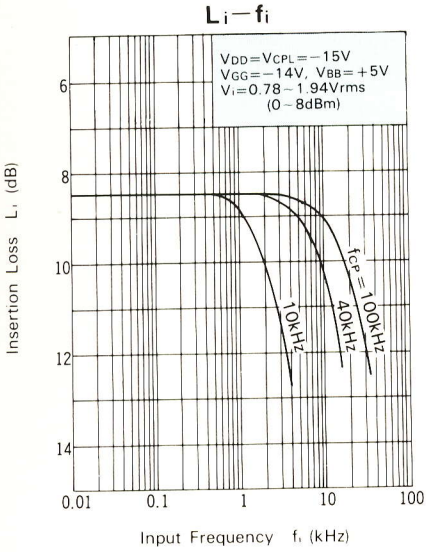
$V_O - V_i$



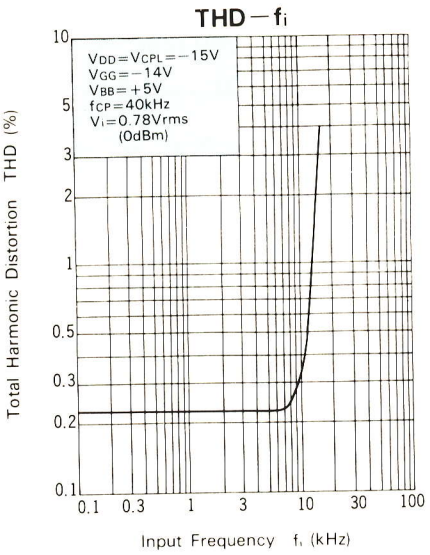
THD − V_i



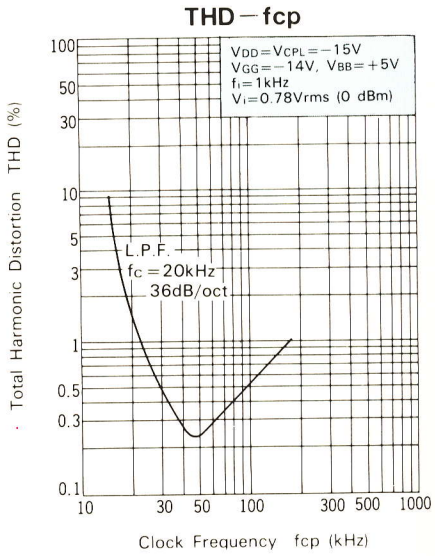
$L_i - f_i$



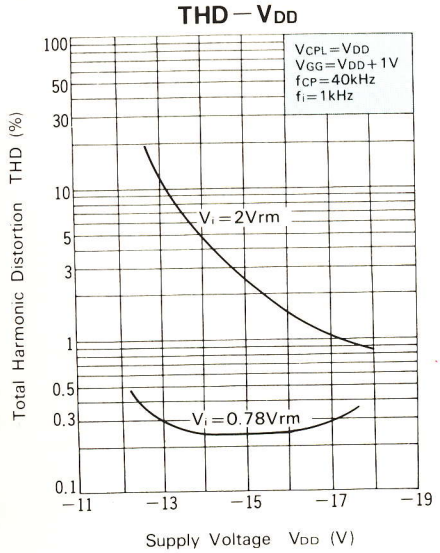
THD − f_i



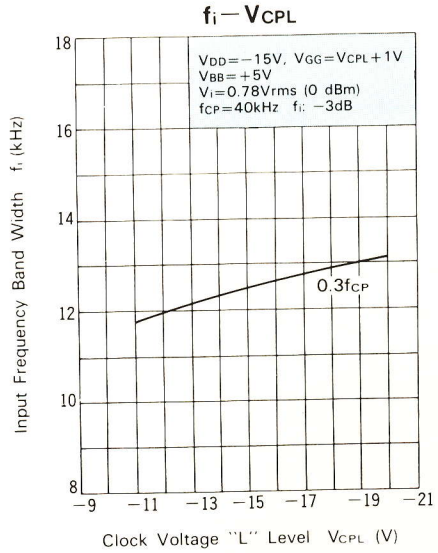
THD − fcp



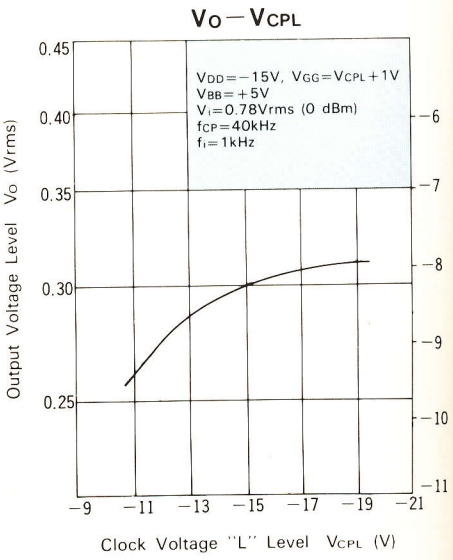
THD − V_{DD}



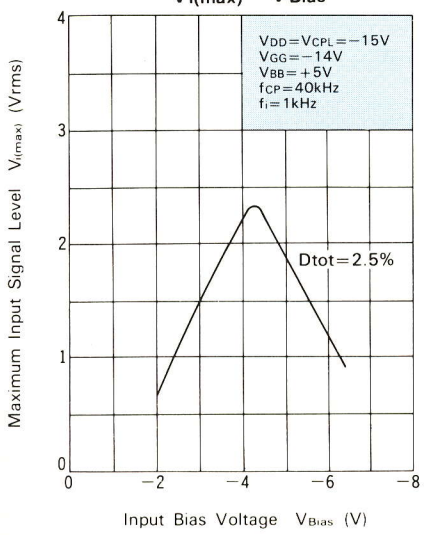
$f_i - V_{CPL}$



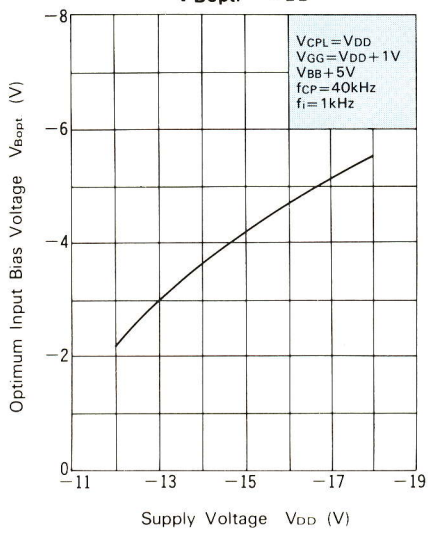
$V_O - V_{CPL}$



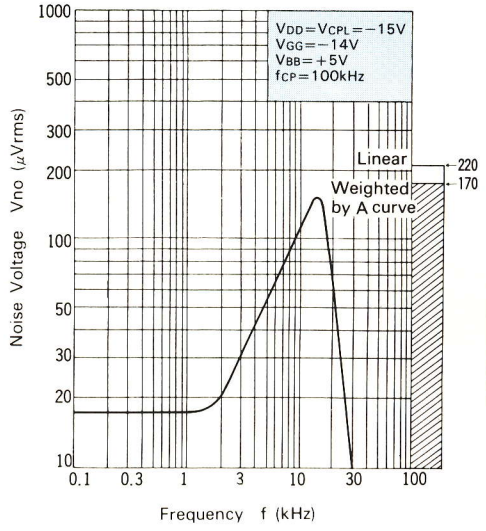
$V_{i(max)} - V_{Bias}$



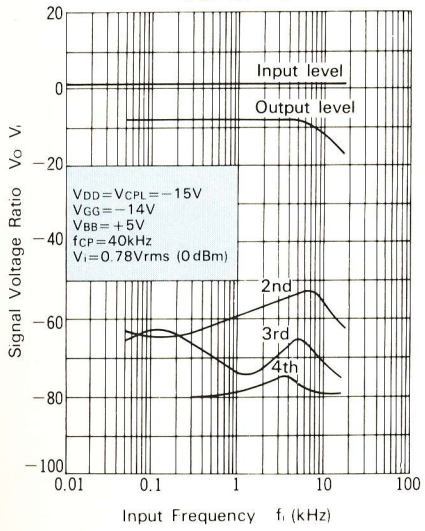
$V_{Bopt.} - V_{DD}$



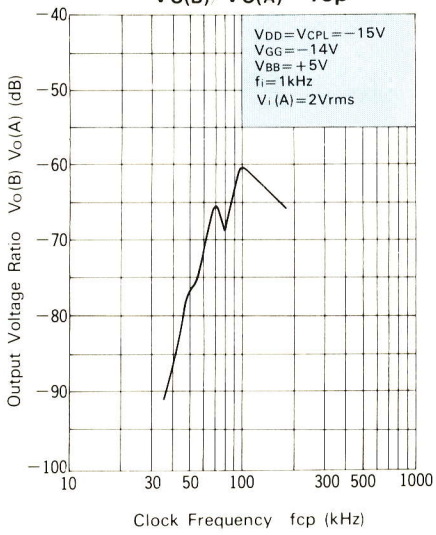
Vno − f



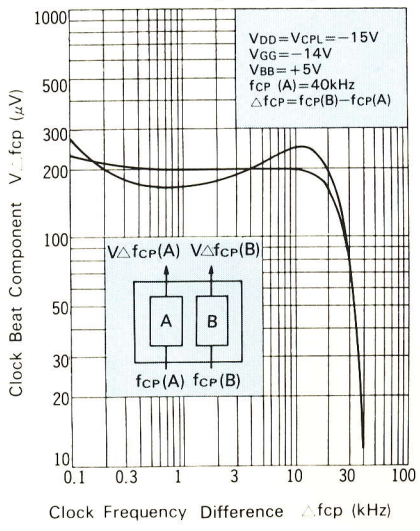
$V_O / V_i - f_i$



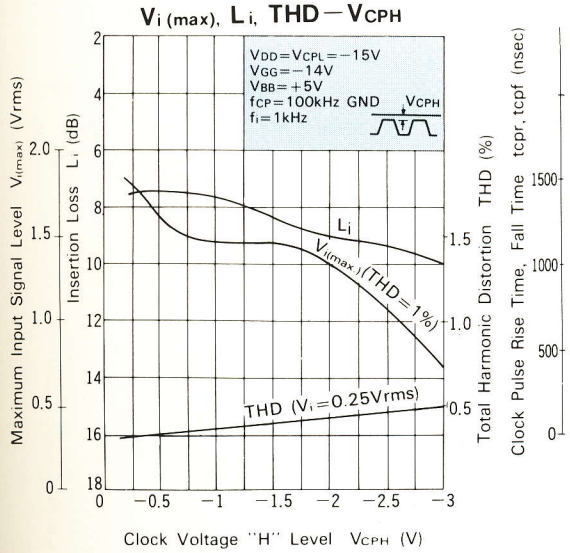
$V_{O(B)} / V_{O(A)} - fcp$



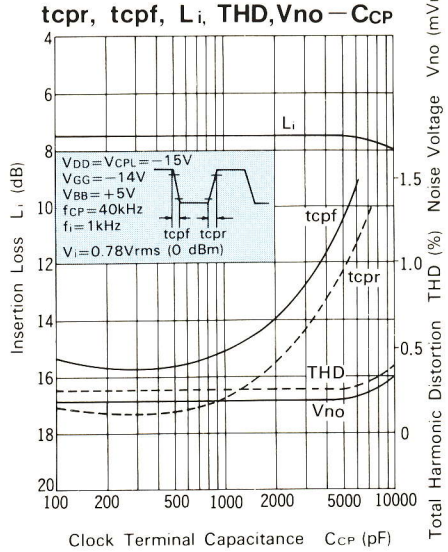
V△fcp − △fcp



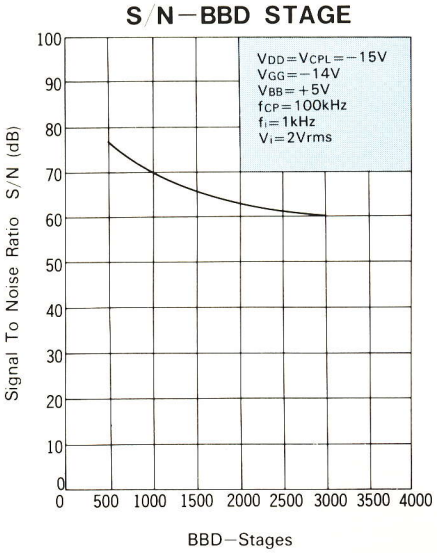
$V_{i\,(max)}$, L_i, THD − V_{CPH}



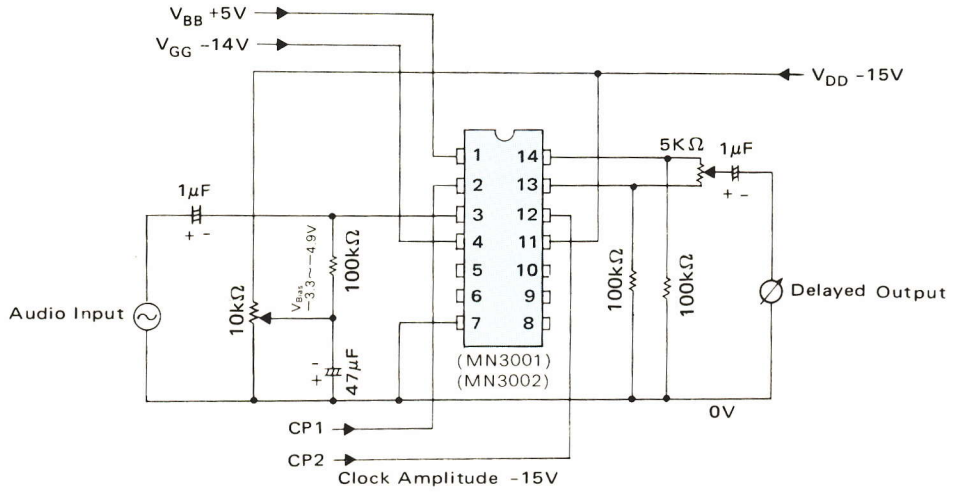
tcpr, tcpf, L_i, THD, Vno − C_{CP}



S/N − BBD STAGE

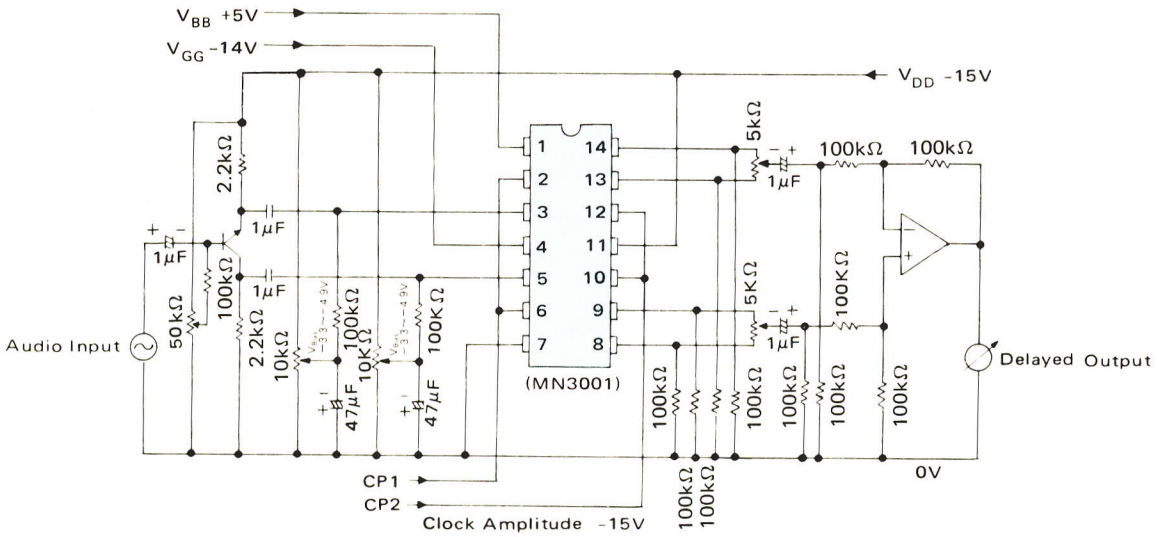


Application Circuit 1



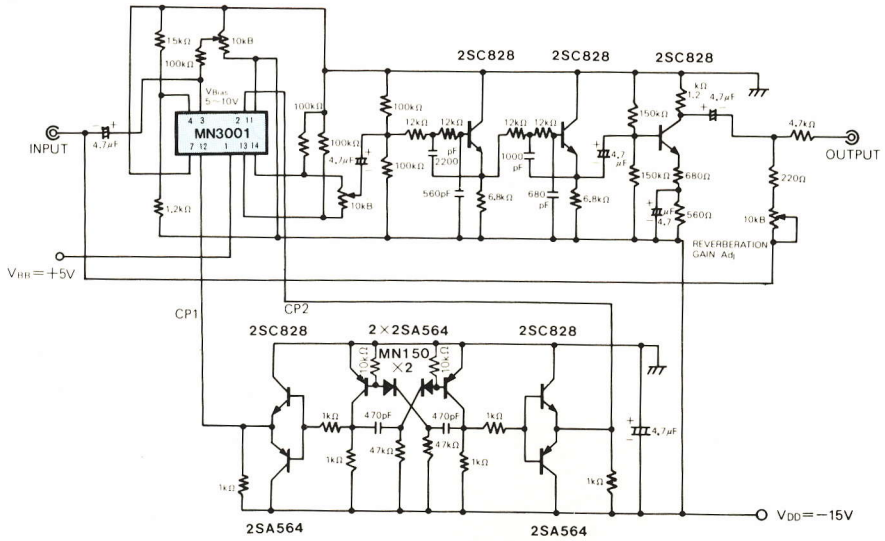
Basic Circuit With Clock Component Cancellation (Single Channel)

Application Circuit 2



Compensation Of DC Level Shift Due To Clock Frequency Change Using Two BBD's
(Dual Channels, Same Clock Phase)

Application Circuit 3



Echo Effect Generation Circuit (Signal Delay Over 10msec.)

MN3003

DUAL-64 STAGE BBD FOR LOW VOLTAGE OPERATION

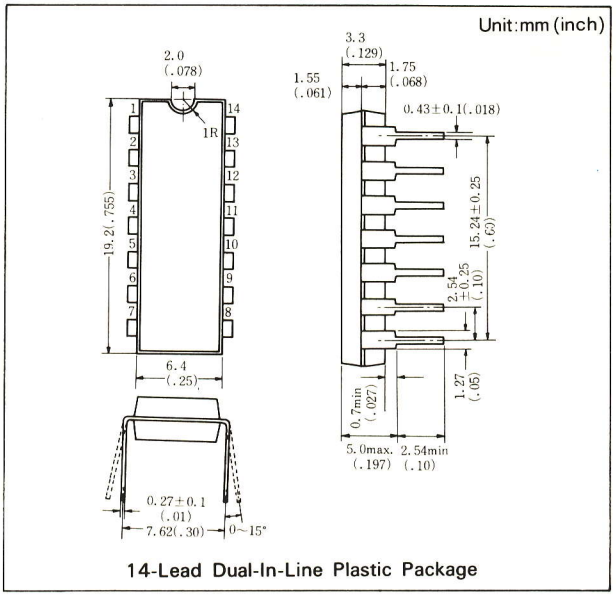
General Description

The MN3003 is a dual 64-stage BBD for low voltage operation (−9V) incorporating a clock generator on a single chip. The 64-stage provides a signal delay of up to 3·2msec.

The dual type contains two identical BBD's on a single chip with independent input, output and common clock terminals, as well as common power supply terminals.

The two identical BBD's on the same chip offer uniform characteristics and space saving advantage when they are used in parallel or series connection.

The clock oscillation frequency is controlled by the external resistor and capacitor connected to CG_1, CG_2 and CG_3 terminals.



14-Lead Dual-In-Line Plastic Package

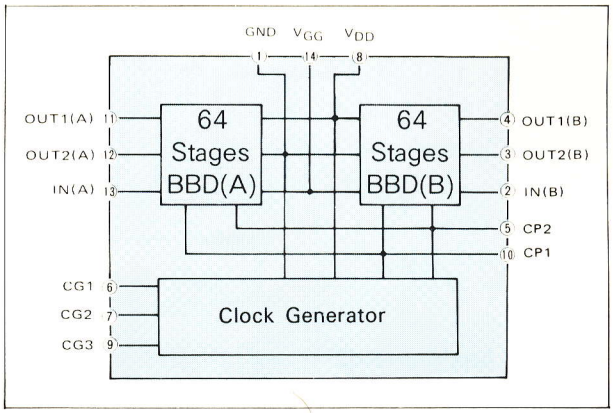
Features:

- Variable delay line in audio frequency range:
  0.16~3.2msec. (64-stage)
  0.32~6.4msec. (64×2-stage)
- Incorporating clock generator circuit.
- Wide frequency response: $f_i \leqq 0.3 \times f_{CP}$
- Wide clock frequency range : 10~200kHz
- Wide dynamic range : S/N=75dB typ.
- Low insertion loss : L_i=3.5dB typ.
- Low noise : Vno=0.14mVrms max.

Applications:

- Vibrato and/or chorus effects in electronic musical instruments.
- Reverberation effect of electronic musical instruments.
- Variable or fixed delay of analog signals.

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−9, V_{DD}+1	V
Signal Delay Time	t_D	0.16~6.4	msec
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	68min	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−15 ~ +0.3	V
Output Voltage	V_O	−15 ~ +0.3	V
Operating Temperature	Topr	−20 ~ +60	°C
Storage Temperature	Tstg	−55 ~ +125	°C

Operating Conditions (Ta=25°C)

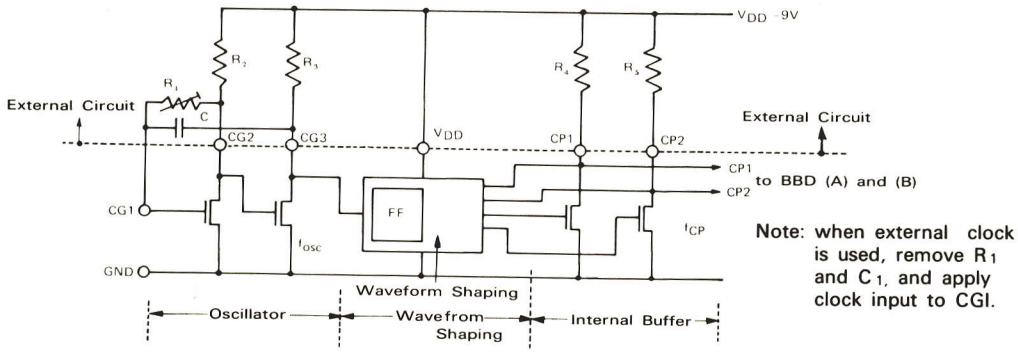
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−8.5	−9	−9.5	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−0.4	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Frequency	f_{CP}		10		200	kHz
Input DC Bias	V_{Bias}		−2.5		−6	V

Electrical Characteristics ($V_{DD}=-9V$, $V_{GG}=-8V$, $R_L=100K\Omega$, $R_2=R_3=22K\Omega$, $R_4=R_5=2.2K\Omega$, $C=100pF$, $f_{CP}=\frac{1}{2}f_{OSC}$ (adjustable by R_1), Ta=25°C)

Item	Symdol	Condition	Min.	Typ.	Max.	Unit
Input Signal Frequency	f_i	f_{CP}=40kHz, V_i=0.8Vrms 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i=1kHz, THD=2.5%			0.8	Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i=1kHz, V_i=0.8Vrms		3.5	7	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i=1kHz, V_i=0.5Vrms		0.5		%
Noise Voltage	Vno	f_{CP}=90kHz, Weighted by "A" curve			0.14	mVrms
Signal to Noise Ratio	S/N		68			dB

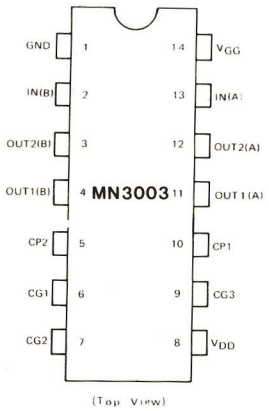
Note: Adjust input DC bias to the optimum value between −2.5 and −6 volts.

Clock Generator Circuit

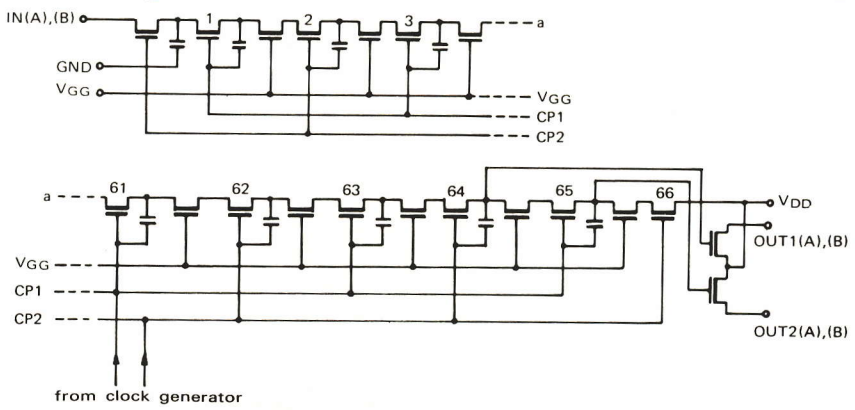


Note: when external clock is used, remove R_1 and C_1, and apply clock input to CGI.

Terminal Assignments

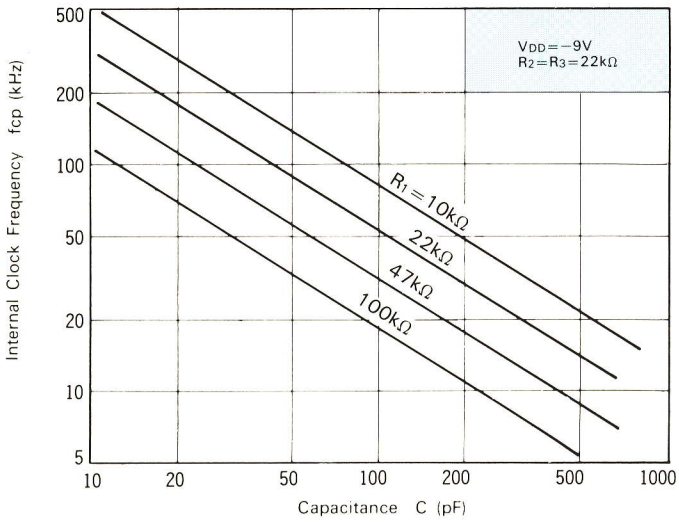


Circuit Diagram

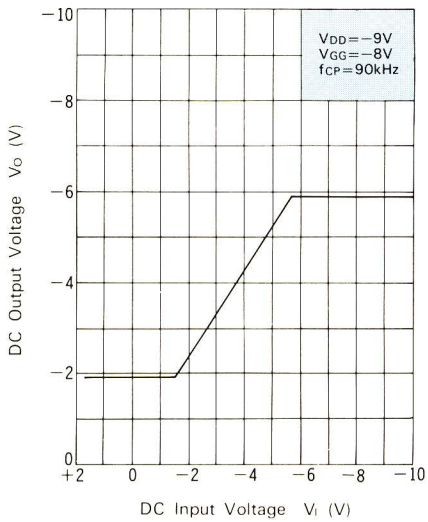


Typical Electrical Characteristic Curves

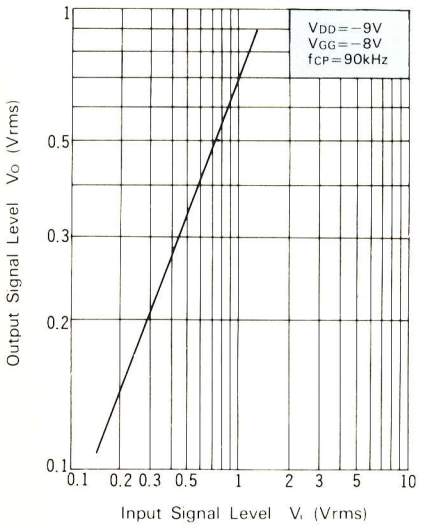
Clock Frequency Characteristics



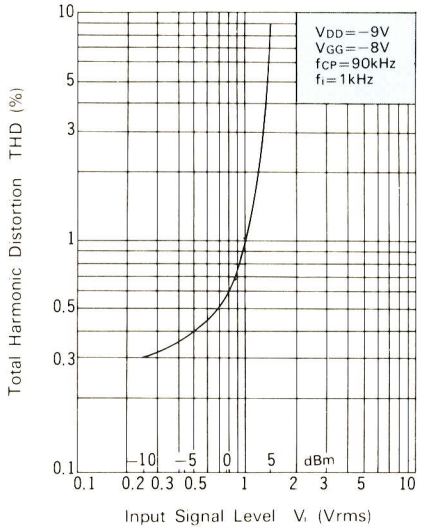
Vo − VI



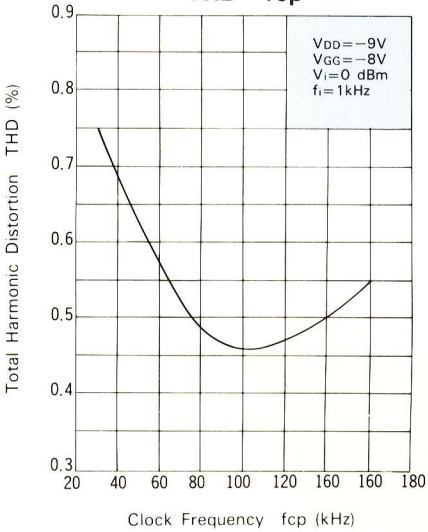
Vo − Vi



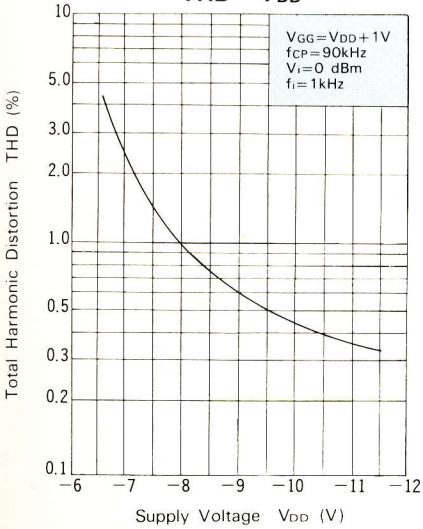
THD − Vi



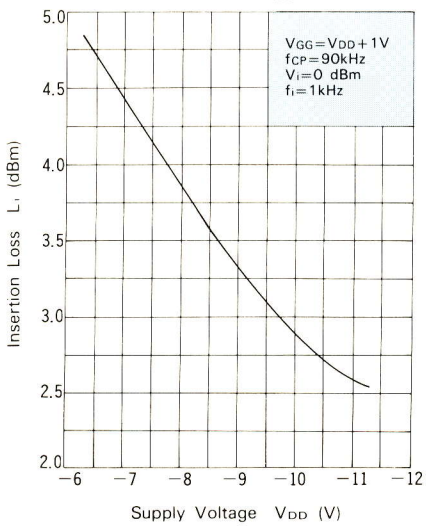
THD − fcp



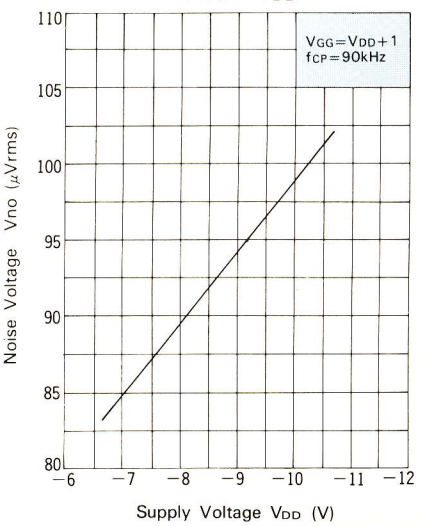
THD − VDD



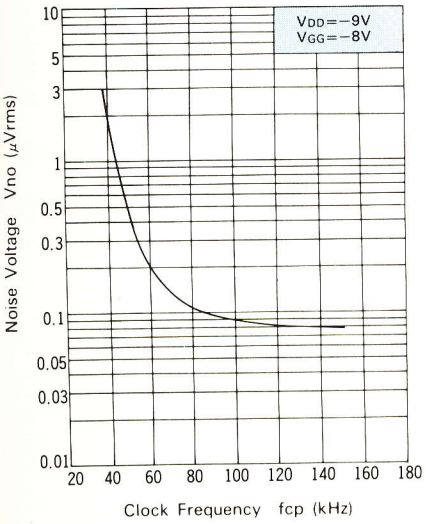
Li − VDD



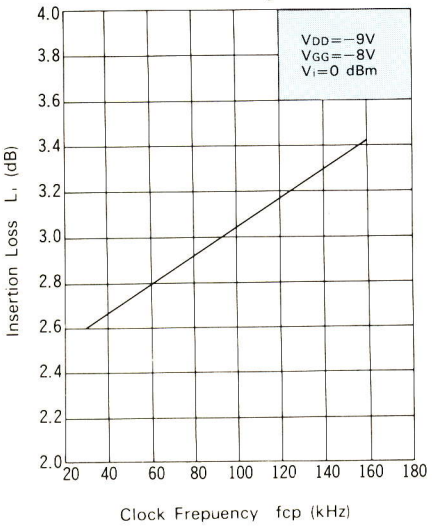
Vno − VDD



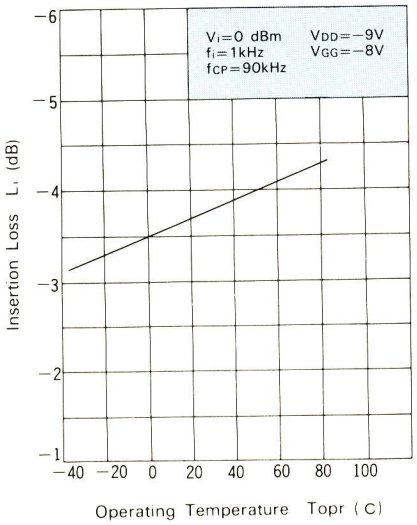
Vno—fcp



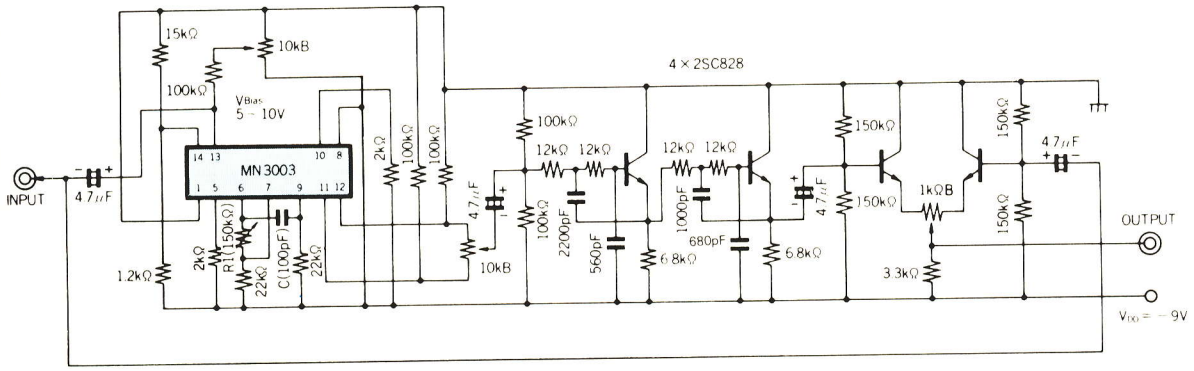
Li—fcp



Li—Topr



Application Circuit



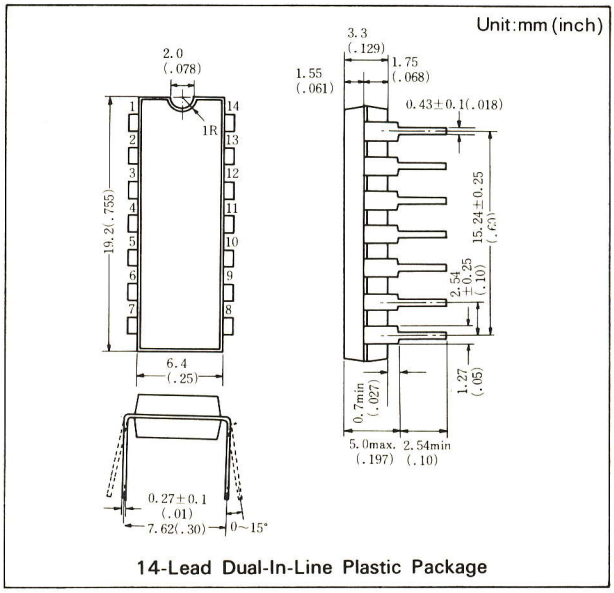
Chorus Effect Generation Circuit (Incorporating Clock Generator)

MN3004

512-STAGE LOW NOISE BBD

General Description

The MN3004 is a 512-stage low noise BBD (Bucket Brigade Device) that provides a signal delay of up to 25.6msec and is suitable for use as variable signal delay lines in audio frequency range.



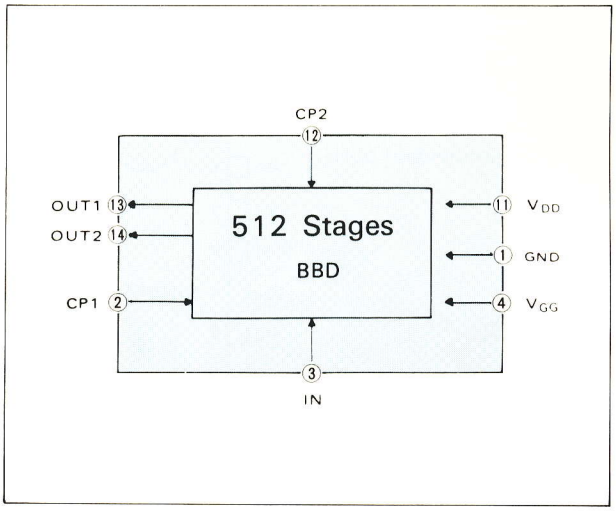
Features:

- Wide range of variable delay time: 2.56~25.6msec.
- Clock component cancellation capability.
- Low insertion loss: $L_i \simeq 1.5$ dB typ.
- Wide dynamic range: S/N≃85 dB typ.
- Wide frequency response: $f_i \leq 0.3 \times f_{CP}$
- Clock frequency range: 10~100kHz.
- Low noise: Vno=0.21mVrms max.
- Total harmonic distortion: THD=0.4% typ.
- P-channel silicon gate, tetrode MOS transistors configuration.
- 8-lead dual-in-line plastic package.

Applications:

- Reverberation effect of echo microphones and stereo equipment.
- Vibrato and/or chorus effects in electronic organs and musical instruments.
- Variable or fixed delay of analog signals.

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	2.56~25.6	msec
Total Harmonic Distortion	THD	0.4	%
Signal to Noise Ratio	S/N	85	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18 ~ +0.3	V
Output Voltage	V_O	−18 ~ +0.3	V
Operating Temperature	Topr	−20 ~ +60	°C
Storage Temperature	Tstg	−55 ~ +125	°C

Operating Conditions (Ta=25°C)

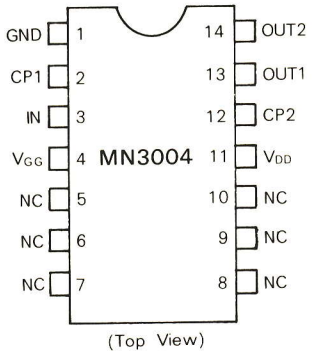
Item	Symdol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−1	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				350	pF
Clock Frequency	f_{CP}		10		100	kHz
Clock Pulse Width *2	tcpw				0.5T *1	
Clock Rise Time *2	tcpr				500	nsec
Clock Fall Time *2	tcpf				500	nsec
Input DC Bias	V_{Bias}		−5		−10	V

Electrical Characteristics (Ta=25°C, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=K\Omega$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		2.56		25.6	msec
Input Signal Frequency	f_i	$f_{CP}=40kHz$, $V_i=1.8Vrms$, 3dB down (0 dB at $f_i=1kHz$)			12	kHz
Input Signal Swing	V_i	$f_{CP}=40kHz$, $f_i=1kHz$, THD=2.5%			1.8	Vrms
Insertion Loss	L_i	$f_{CP}=40kHz$, $f_i=1kHz$, $V_i=1.8Vrms$		1.5	4.8	dB
Total Harmonic Distortion	THD	$f_{CP}=40kHz$, $f_i=1kHz$, $V_i=1Vrms$		0.4		%
Noise Voltage	Vno	$f_{CP}=100kHz$ Weighted by "A" curve			0.21	mVrms
Signal to Noise Ratio	S/N		75	85		dB

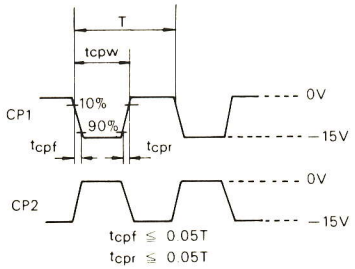
*1 T=1 fcp (Clock Period)
*2 Clock Pulse Waveforms

Terminal Assignments

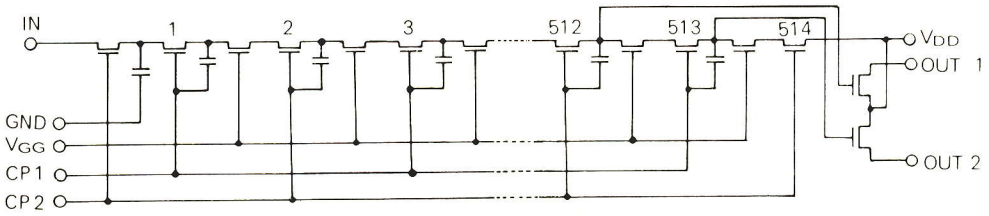


(Top View)

Clock Pulse Waveforms

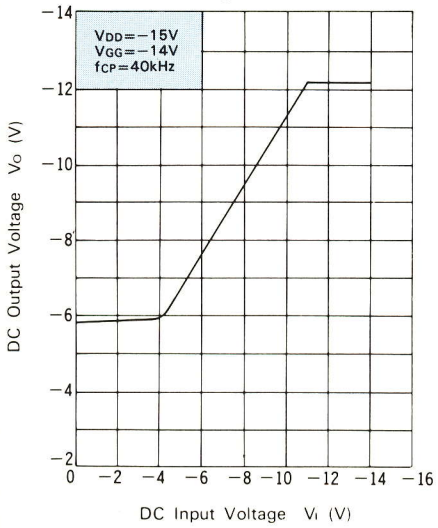


Circuit Diagram

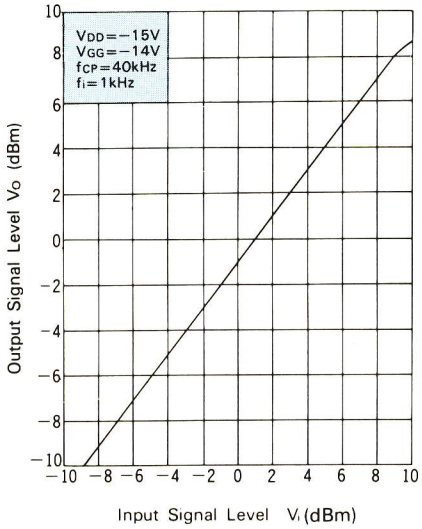


Typical Electrical Characteristic Curves

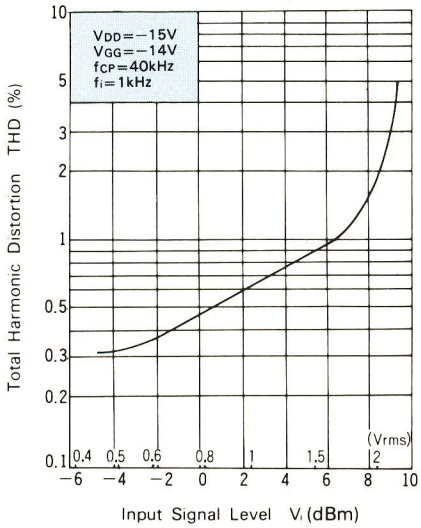
$V_O - V_I$



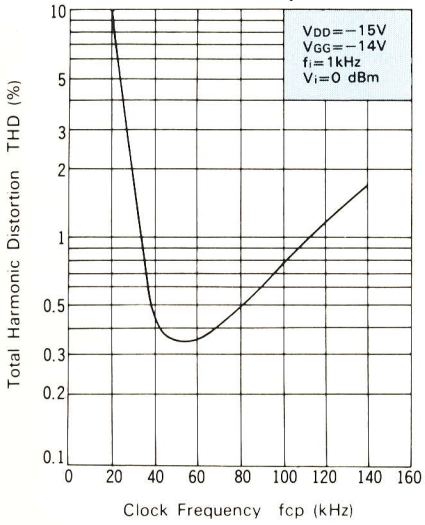
$V_O - V_i$



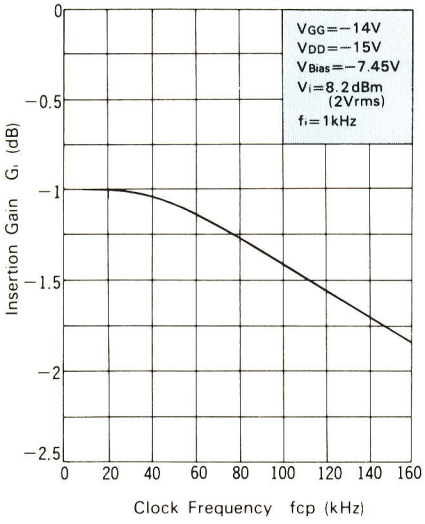
$THD - V_i$



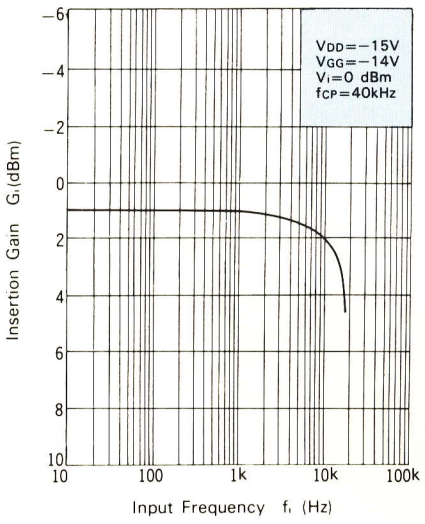
$THD - f_{CP}$



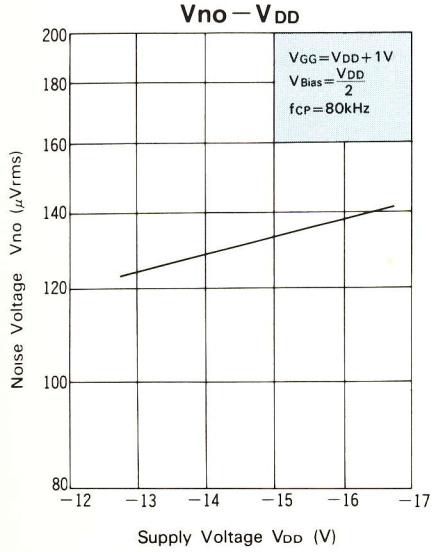
$G_i - f_{CP}$



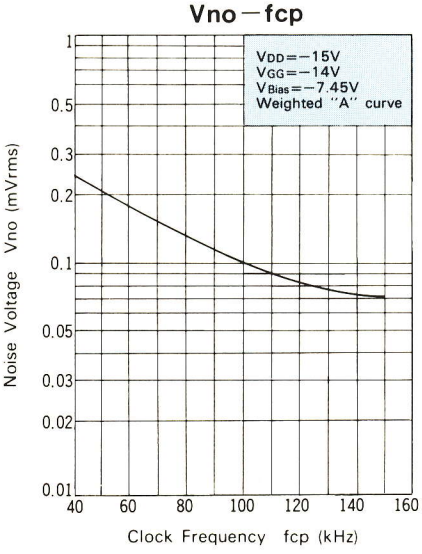
$G_i - f_i$



$V_{no} - V_{DD}$

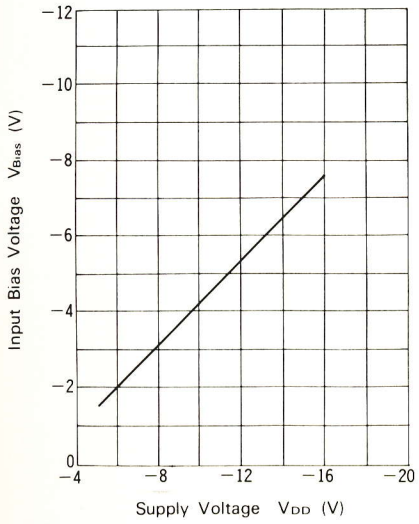


$V_{no} - f_{CP}$

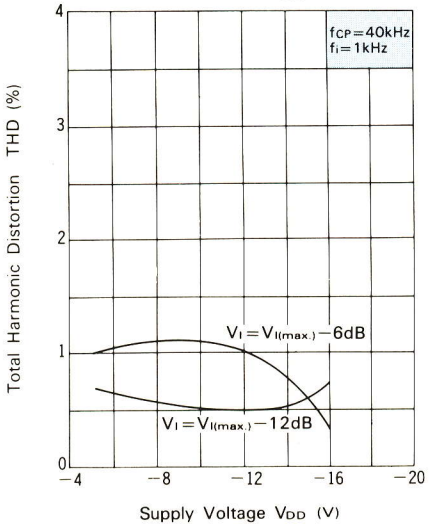


Supply Voltage Characteristics

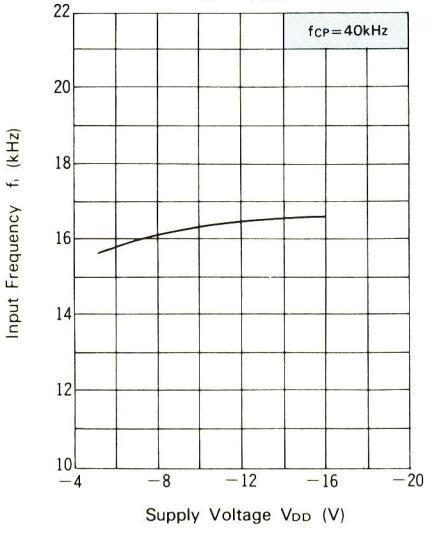
$V_{Bias} - V_{DD}$



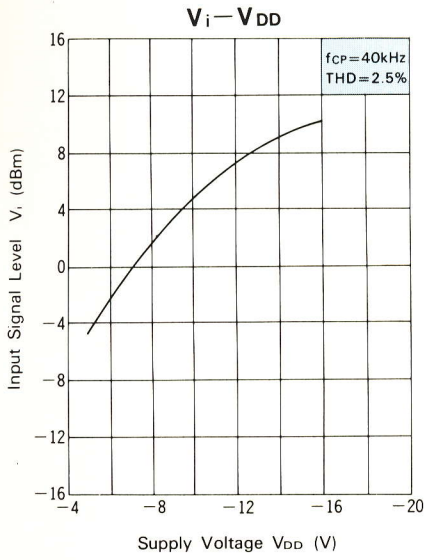
$THD - V_{DD}$



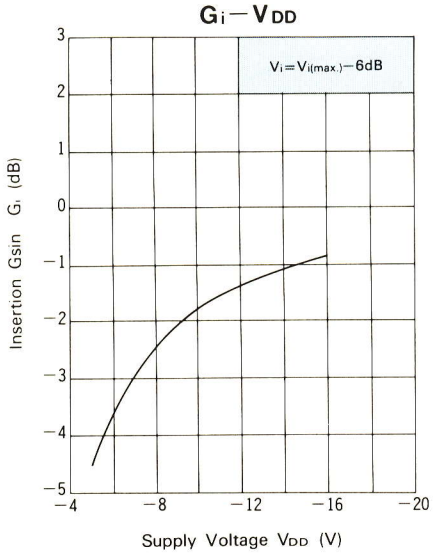
$f_i - V_{DD}$



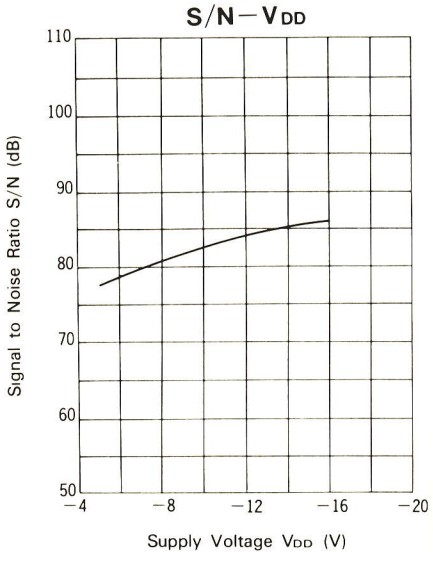
$V_i - V_{DD}$



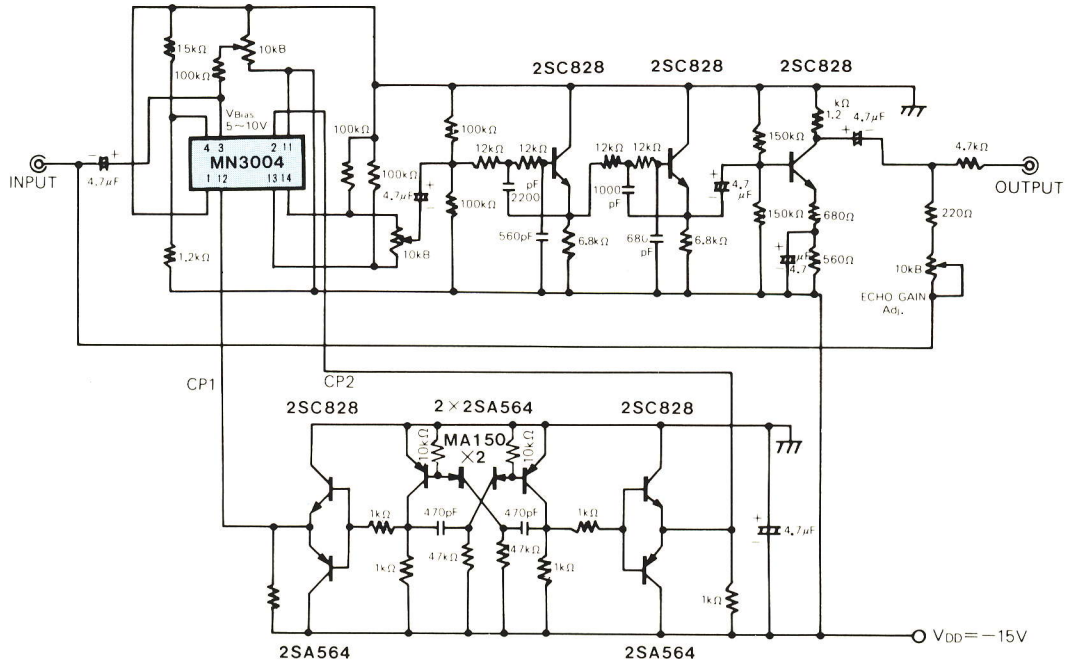
$G_i - V_{DD}$



$S/N - V_{DD}$



Application Circuit



Echo Effect Generation Circuit (Signal Delay Over 10msec.)

MN3005

4096-STAGE LOW NOISE BBD

General Description

The MN3005 is a 4096-stage long delay BBD (Bucket Brigade Device) that provides a signal delay of up to 204.8-msec and is suitable for use as variable signal delay lines in audio frequency range.

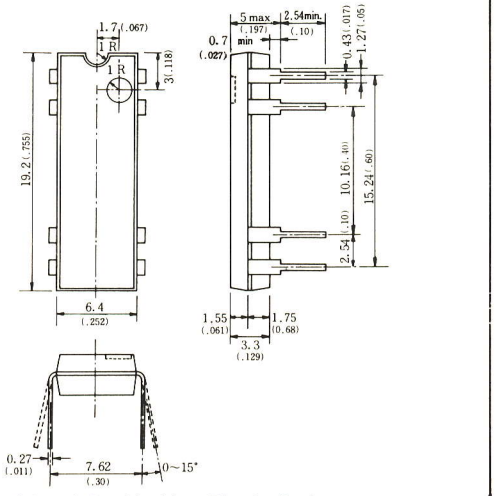
Features:

- Wide range of variable delay time : 20.48～204.8msec.
- Clock component cancellation capability.
- No insertion loss : $L_i \simeq 0$ dB typ.
- Wide dynamic range : S/N≃75dB typ.
- Wide frequency response : $f_i \leq$ 10kHz.
- Low distortion : THD=1% typ. (V_i=0.78Vrms)
- Clock frequency range : 10～100kHz.
- P-channel silicon gate, tetrode MOS transistors configuration.
- 8-lead dual-in-line plastic package.

Applications:

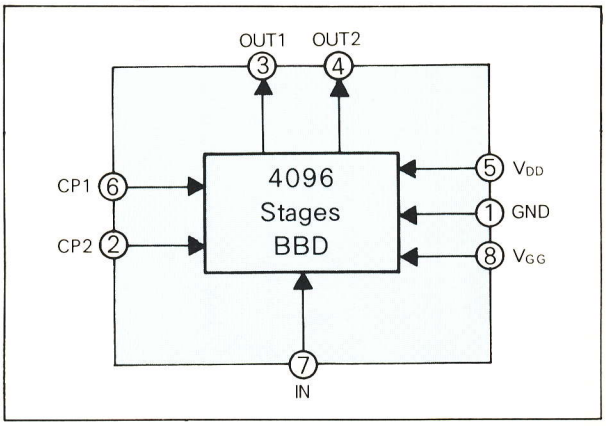
- Reverberation effect of echo microphones and stereo equipment.
- Chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems : etc.

Unit : mm(inch)



8-Lead Dual-In-Line Plastic Package

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	20.48～204.8	msec
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18~+0.3	V
Output Voltage	V_O	−18~+0.3	V
Operating Temperature	Topr	−20~+ 60	℃
Storage Temperature	Tstg	−55~+125	℃

Operating Conditions (Ta=25℃)

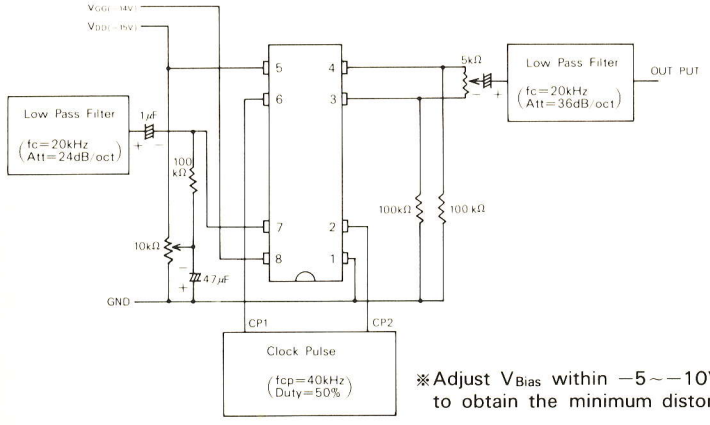
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}		0		−1	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				2800	pF
Clock Frequency	f_{cp}		10		100	kHz
Clock Pulse Width *2	t_{cpw}	Test Circuit			0.5T*1	
Clock Rise Time *2	t_{cpr}	Test Circuit			500	nsec
Clock Fall Time *2	t_{cpf}	Test Circuit			500	nsec
Input DC Bias Voltage	V_{Bias}		−5		−10	V

*1 T=1/fcp *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25℃, V_{DD}=V_{CPL}=−15V, V_{CPH}=0V, V_{GG}=−14V, R_L=100kΩ)

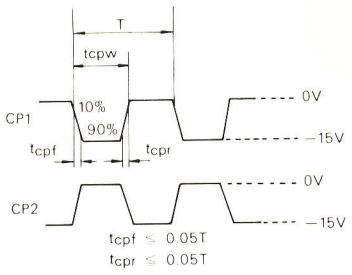
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		20.48		204.8	msec
Input Signal Frequency	f_I	f_{cp}=40kHz, V_I=1.3Vrms, Output Attenuation ≦ 3dB(0dB at f_I=1kHz)			10	kHz
Input Signal Swing	V_i	f_{cp}=40kHz, f_I=1kHz, THD=2.5%			1.2	Vrms
Insertion Loss	L_I	f_{cp}=40kHz, f_I=1kHz, V_I=1.2Vrms		0	4	dB
Total Harmonic Distortion	THD	f_{cp}=40kHz, f_I=1kHz, V_I=0.78Vrms		1	2.5	%
Noise Voltage	Vno	f_{cp}=100kHz Weighted by "A" curve			0.4	mVrms
Signal to Noise Ratio	S/N			75		dB

Test Circuit

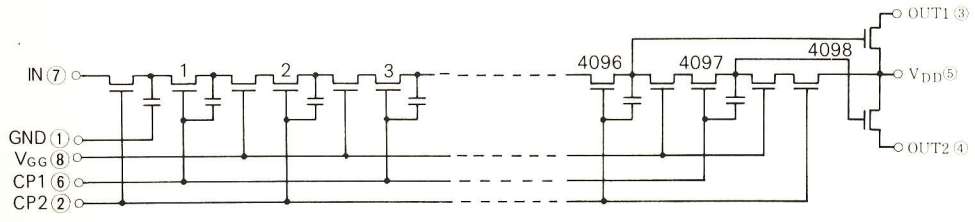


※Adjust V_{Bias} within −5~−10V so as to obtain the minimum distortion.

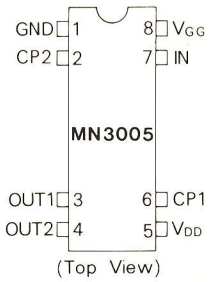
Clock Pulse Waveforms



Circuit Diagram

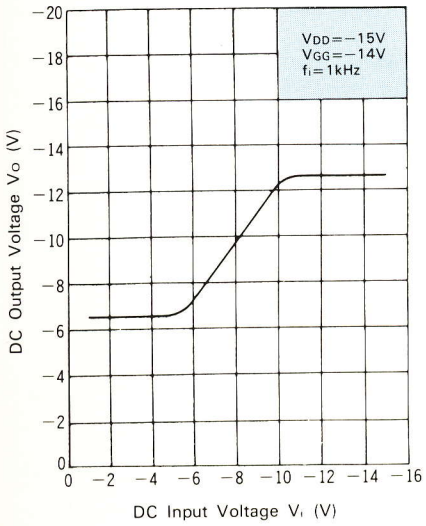


Terminal Assignments

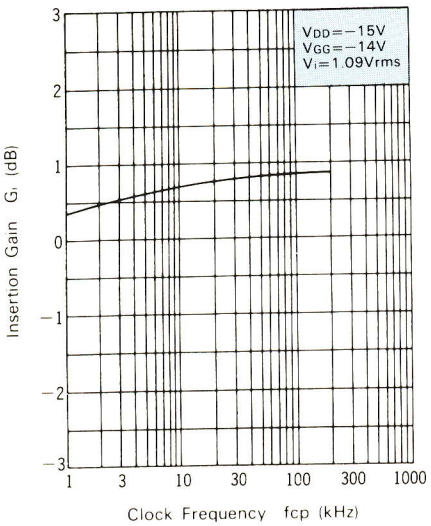


Typical Electrical Characteristic Curves

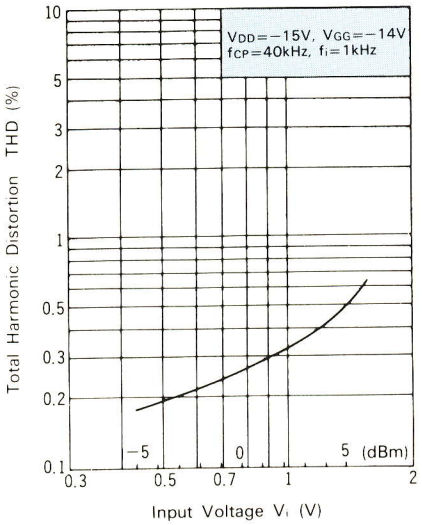
$V_O - V_I$



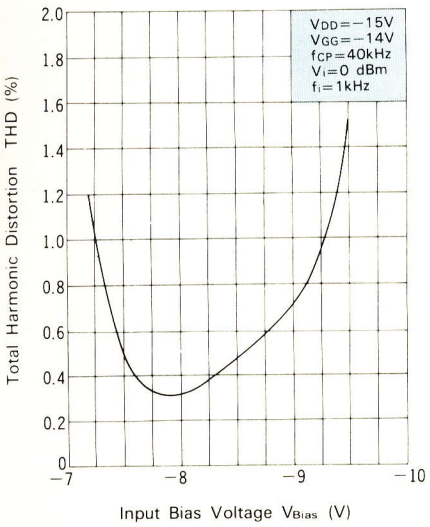
$G_i - f_{cp}$



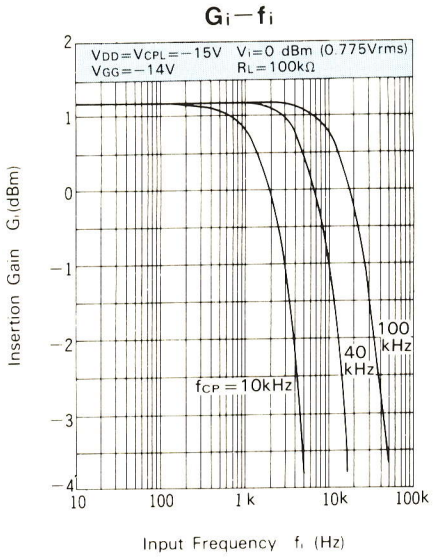
$THD - V_i$



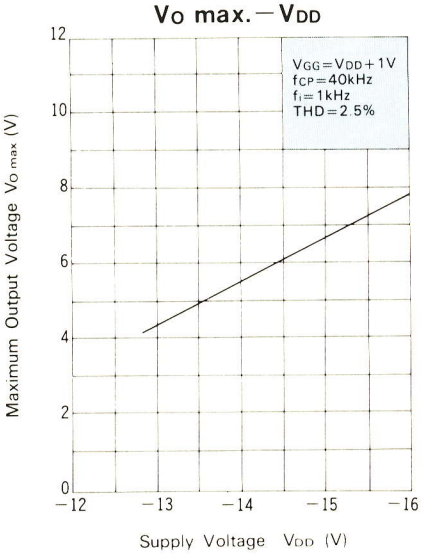
$THD - V_{Bias}$



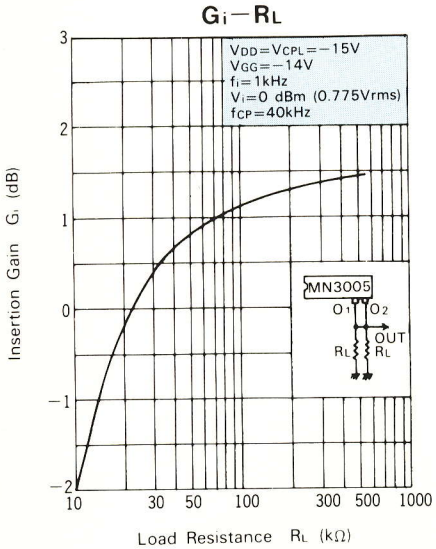
$G_i - f_i$



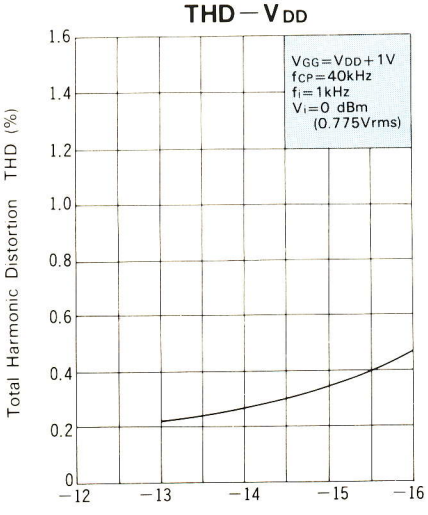
V_O max. $- V_{DD}$



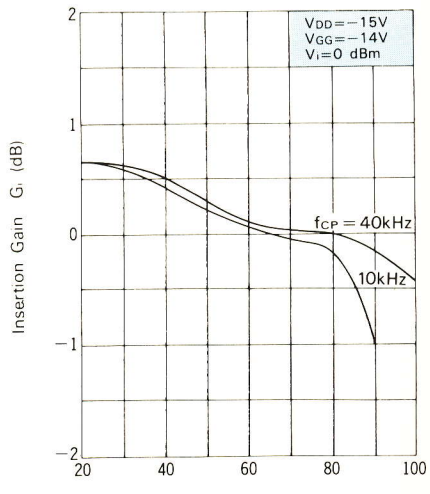
$G_i - R_L$



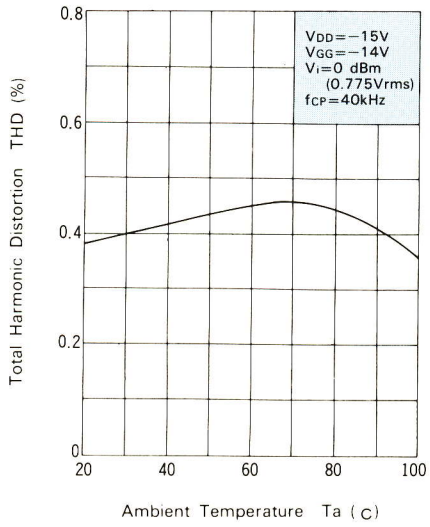
$THD - V_{DD}$



$G_i - Ta$

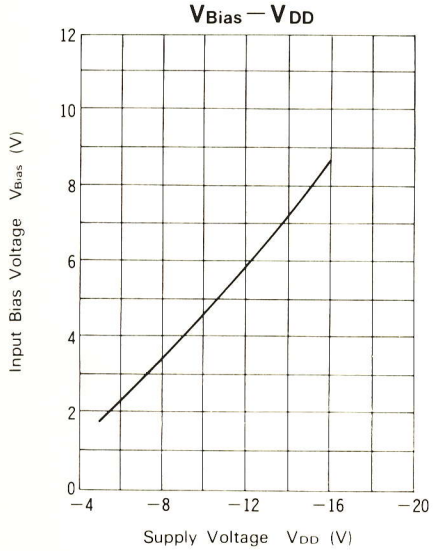


THD — Ta

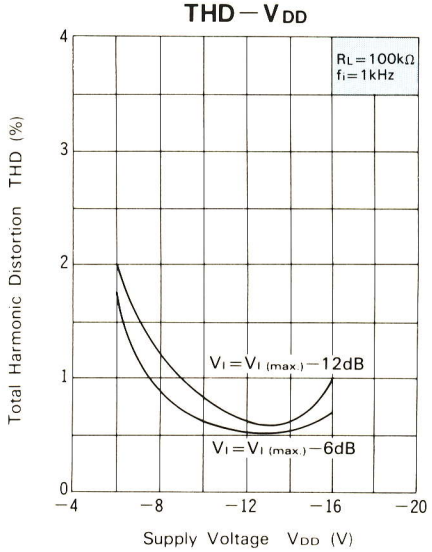


Supply Voltage Characteristics

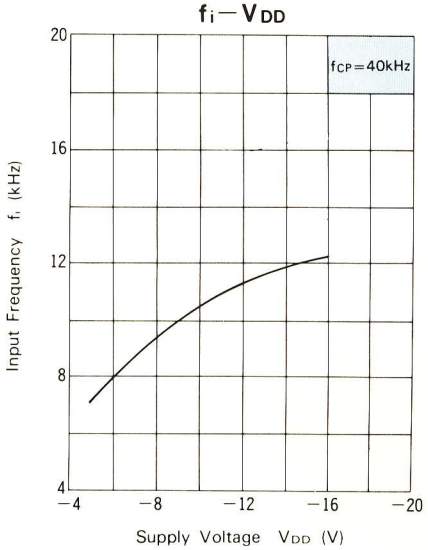
VBias — VDD



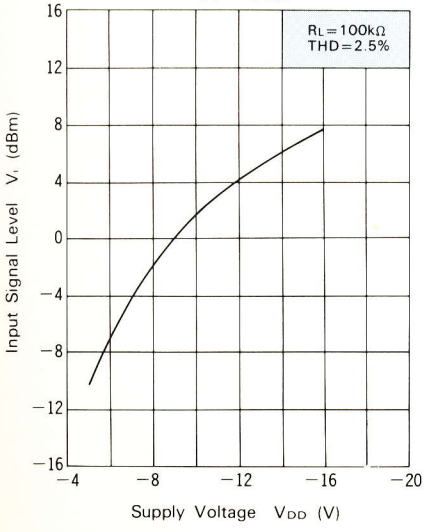
THD — VDD



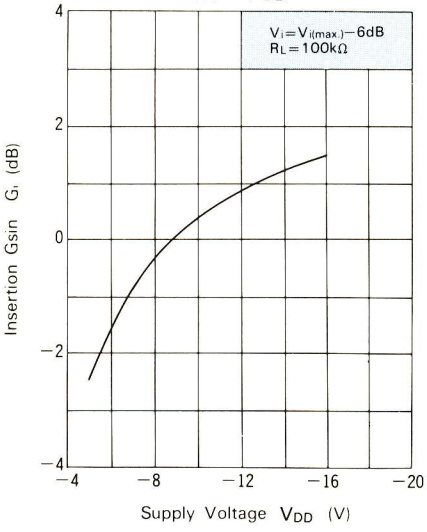
fi — VDD



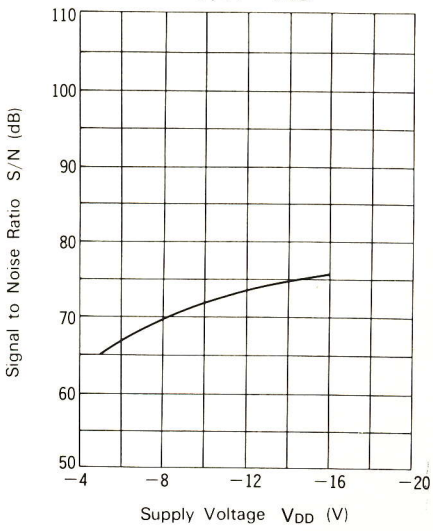
Vi — VDD



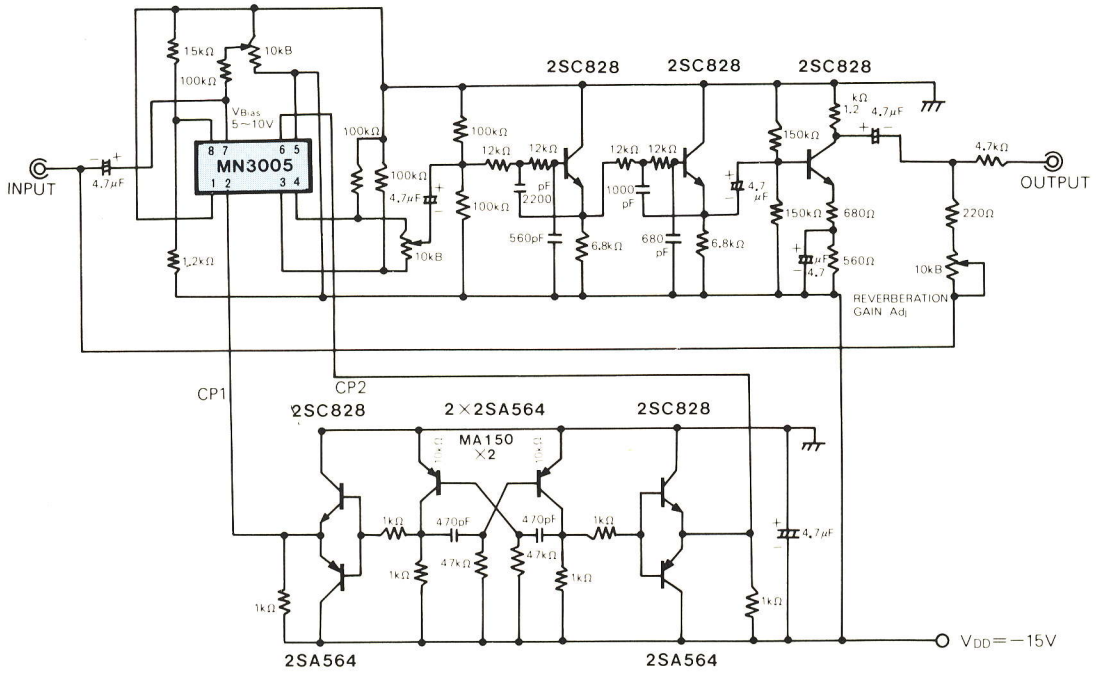
Gi — VDD



S/N — VDD



Application Circuit



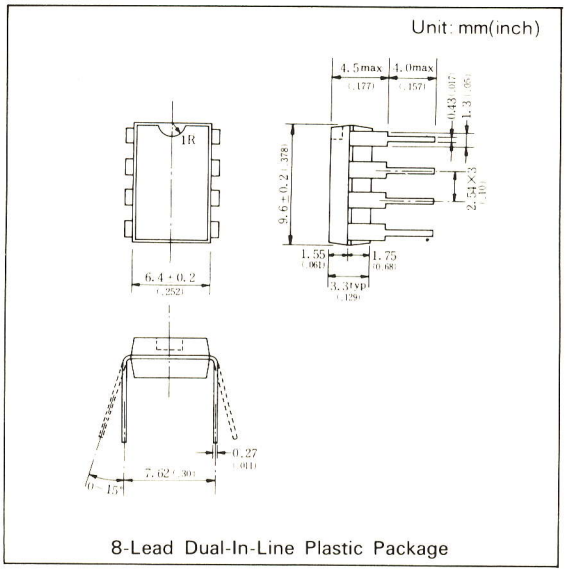
Reverberation Effect Generation Circuit (Signal Delay Over 100msec.)

MN3006

128-STAGE LOW NOISE BBD

General Description

The MN3006 is a 128-stage Low Noise BBD (Bucket Brigade Device) that provides a signal delay of up to 6.4-msec. The typical applications are vibrato and chorus effects in electronic organs and musical instruments.



8-Lead Dual-In-Line Plastic Package

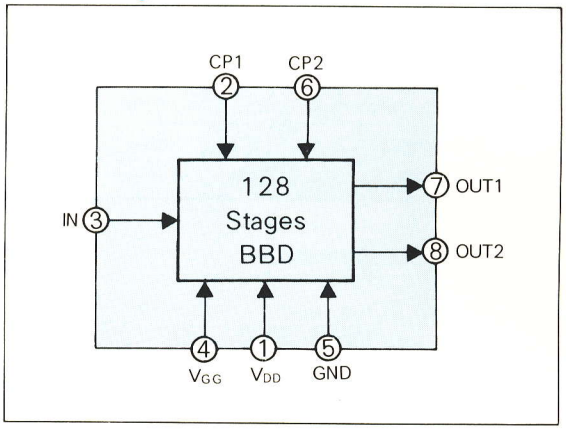
Features:

- Variable delay time : 0.32~6.4msec.
- Clock component cancellation capability.
- Low insertion loss : $L_i \simeq 0$ dB typ.
- Wide dynamic range : S/N≃90dB typ.
- Wide frequency response : $f_i < 15$kHz.
- Low Noise: Vno=0.2mVrms max.
- Total harmonic distortion : THD=0.2% typ. (V_i=0.78Vrms)
- Clock frequency range : 10~200kHz.
- P-channel silicon gate, tetrode MOS transistors configuration.
- 8-lead dual-in-line plastic package.

Applications:

- Vibrato and / or chorus effects in electronic organs and musical instruments.
- Variable or fixed delay of analog signals.

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	0.32~6.4	msec
Total Harmonic Distortion	THD	0.2	%
Signal to Noise Ratio	S/N	90	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Terminal Voltage	V_{DD} V_{GG} V_{CP} V_I	−18~+0.3	V
Output Voltage	V_O	−18~+0.3	V
Operating Temperature	Topr	−20~+60	°C
Storage Temperature	Tstg	−55~+125	°C

Operating Conditions (Ta=25°C)

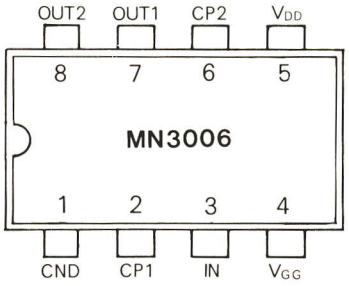
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD} +1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			100	pF
Clock Frequency	f_{CP}	10		200	kHz
Clock Pulse Width *2	t_{CPW}			0.5T *1	
Clock Rise Time *2	t_{CPr}			500	nsec
Clock Fall Time *2	t_{CPf}			500	nsec
Clock Cross Point	V_X	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25°C, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

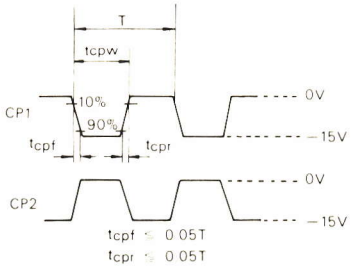
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		0.32		6.4	msec
Input Signal Frequency	f_i	f_{CP}=40kHz, V_i=1.8Vrms, 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i=1kHz, THD=2.5%			1.8	Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i=1kHz, V_i=1.8Vrms	−4	0	4	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.2	2.5	%
Noise Voltage	Vno	f_{CP}=100kHz, Weighted by "A" curve		0.08	0.2	mVrms
Signal to Noise Ratio	S/N	Maximum output voltage to noise voltage		90		dB

Terminal Assignments

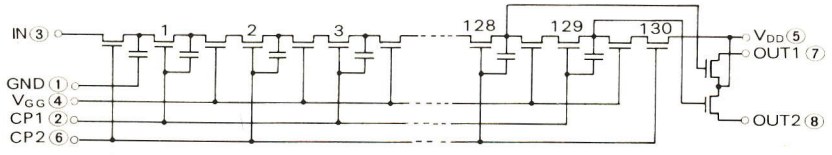


(Top View)

Clock Pulse Waveforms

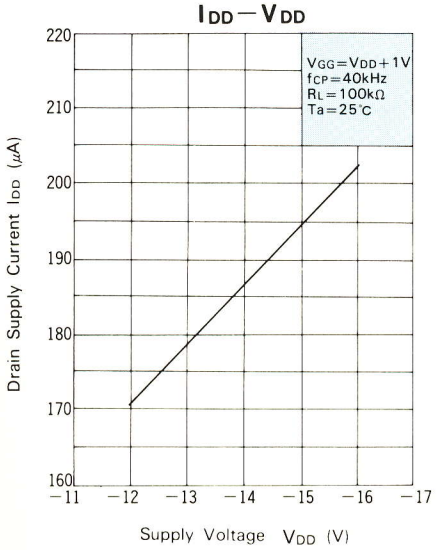


Circuit Diagram

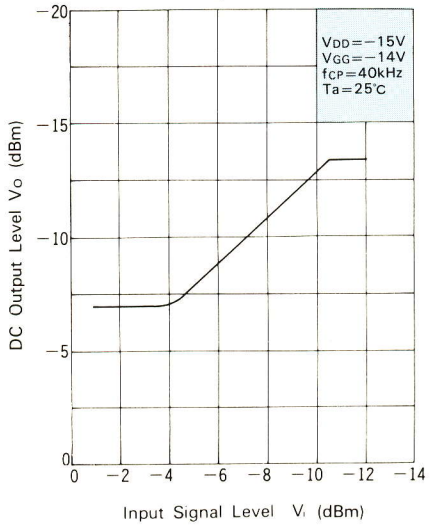


Typical Electrical Characteristic Curves

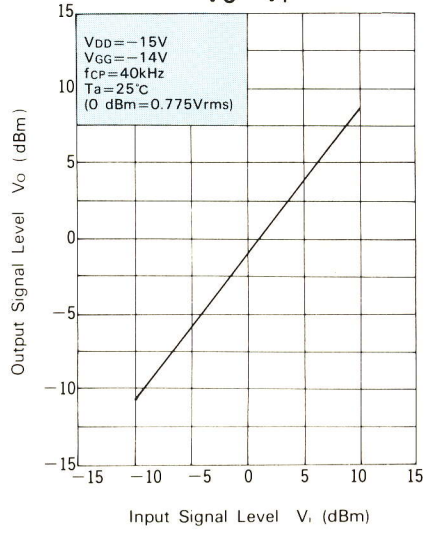
$I_{DD} - V_{DD}$



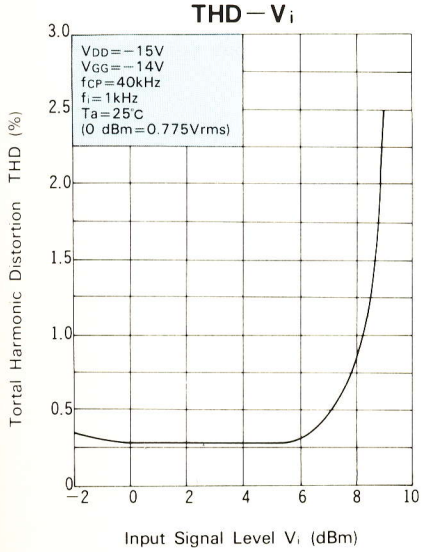
$V_O - V_I$



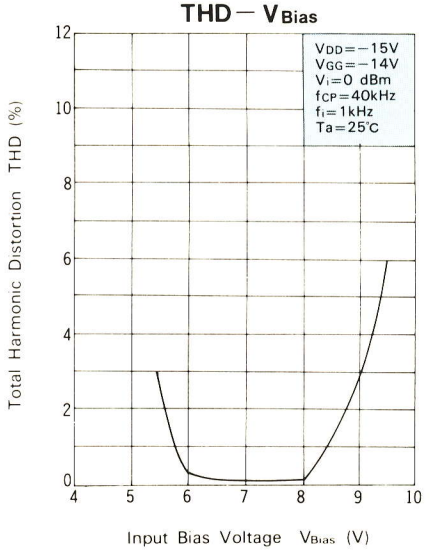
$V_O - V_i$



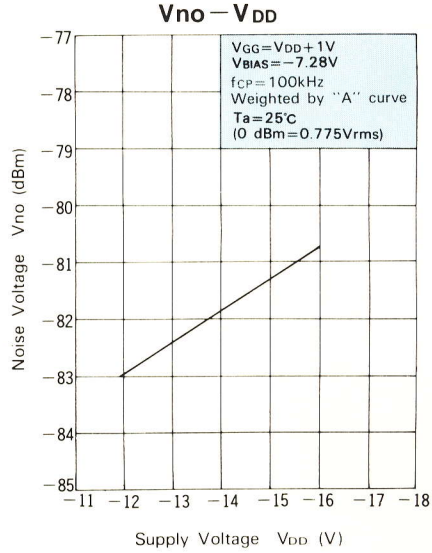
THD − V_i



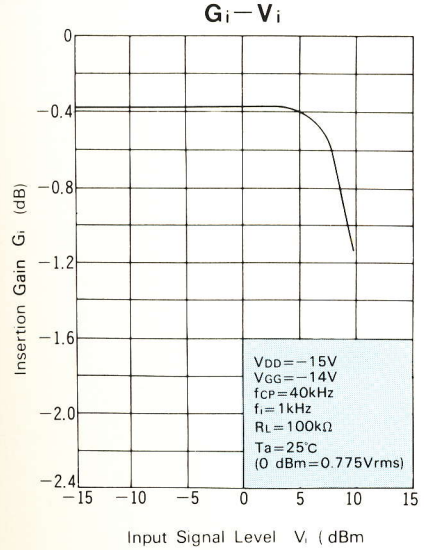
THD − V_{Bias}



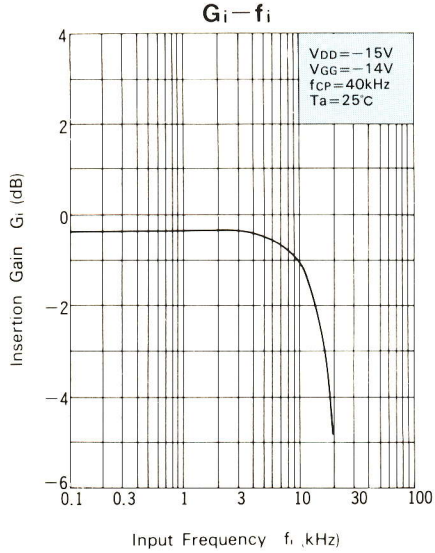
Vno − V_{DD}



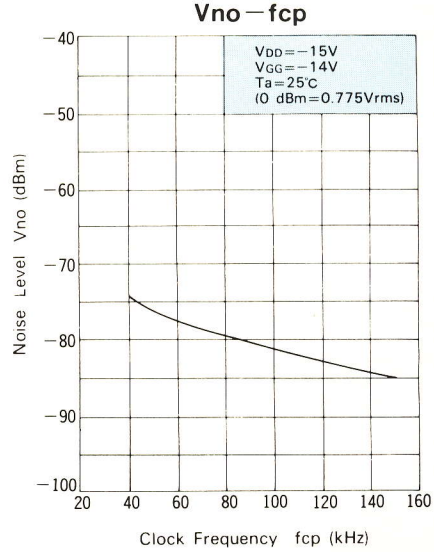
$G_i - V_i$



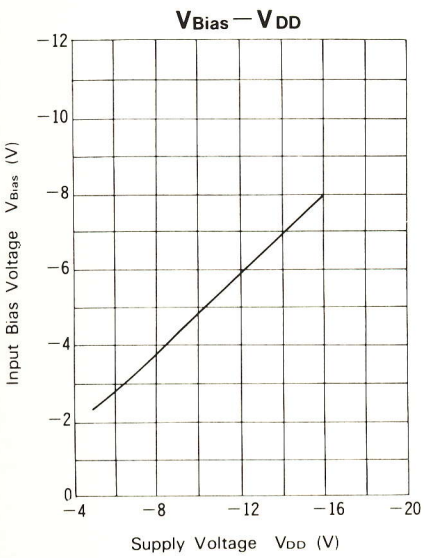
$G_i - f_i$

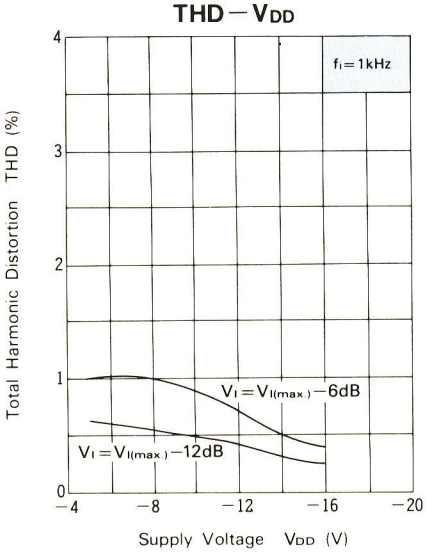


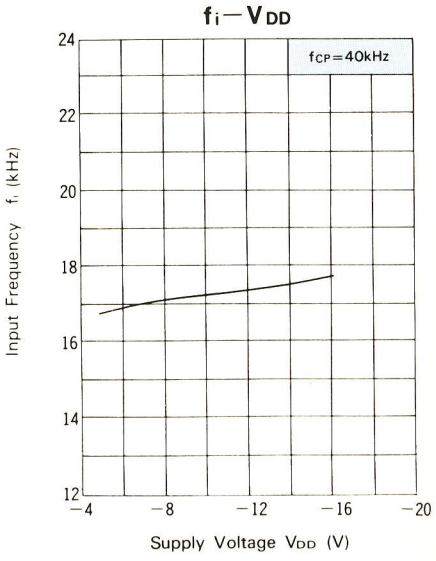
Vno − fcp

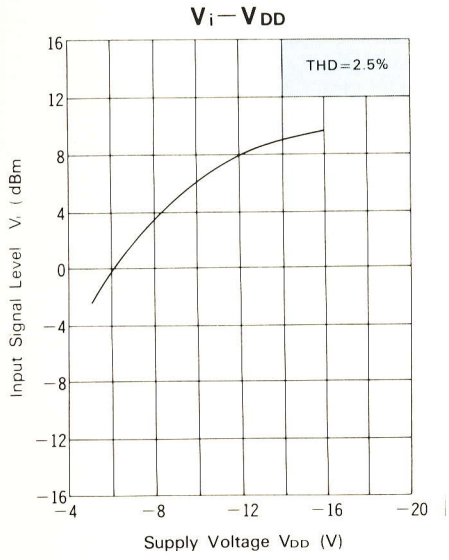


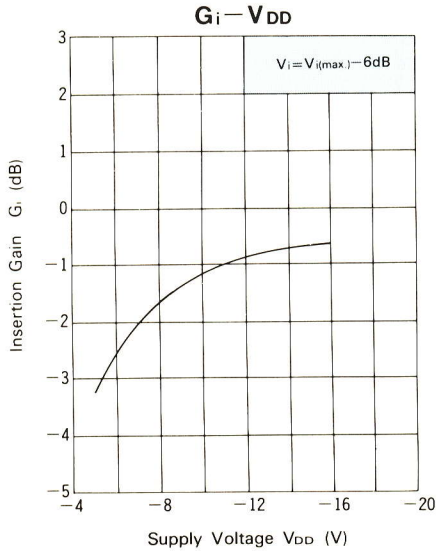
Supply Voltage Characteristics

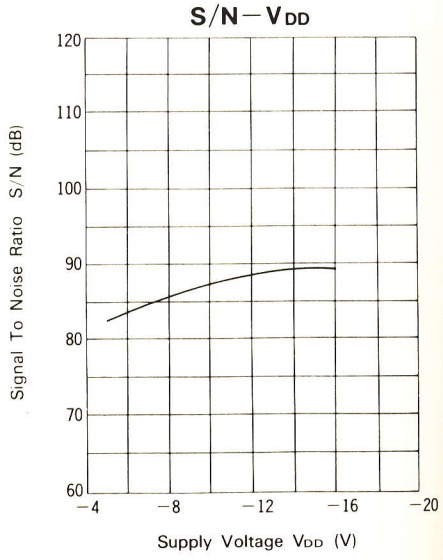




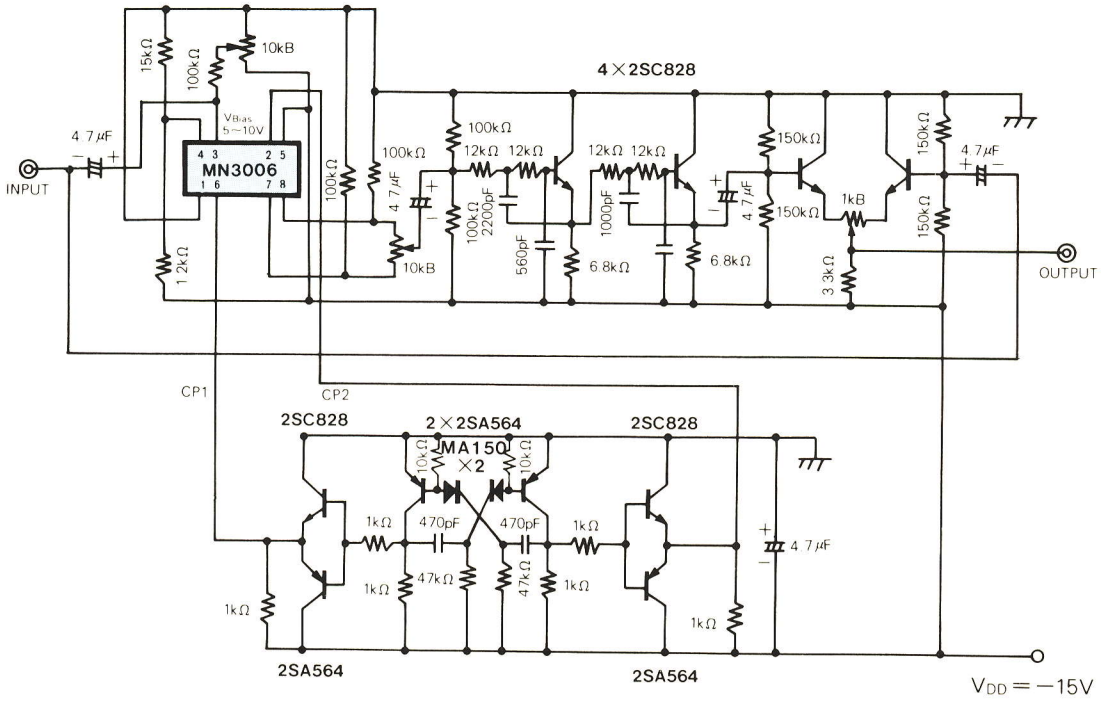








Application Circuit



Chorus Effect Generation Circuit

MN3007

1024-STAGE LOW NOISE BBD

General Description

The MN3007 is a 1024-stage long delay BBD (Bucket Brigade Device) that provides a signal delay of up to 51.2msec. The MN3007 is particularly suitable for use as variable signal delay lines in audio frequency range.

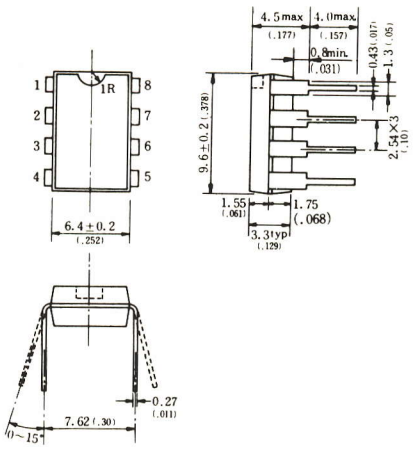
Features:

- Wide range of variable delay time: 5.12~51.2msec.
- Clock component cancellation capability.
- No insertion loss: $L_i \simeq 0$ dB typ.
- Wide dynamic range: S/N $\simeq$ 80 dB typ.
- Wide frequency response: $f_i < 12$kHz.
- Total harmonic distortion: THD=0.5% typ. (V_i=0.78Vrms)
- Clock frequency range: 10~100kHz.
- P-channel silicon gate, tetrode MOS transistors configuration
- 8-lead dual-in-line plastic package.

Applications:

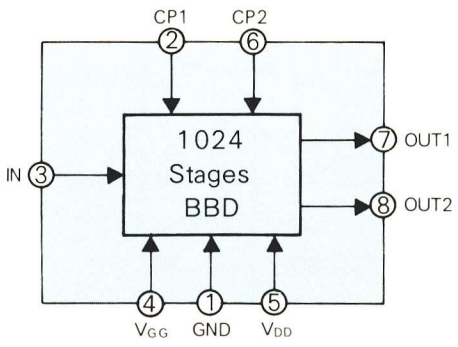
- Reverberation effect of echo microphones and stereo equipment.
- Chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.

Unit : mm (inch)



8-Lead Dual-In-Line Plastic Package

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	5.12~51.2	msec
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	80	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18~+0.3	V
Output Voltage	V_O	−18~+0.3	V
Operating Temperature	Topr	−20~+60	°C
Storage Temperature	Tstg	−55~+125	°C

Operating Conditions (Ta=25°C)

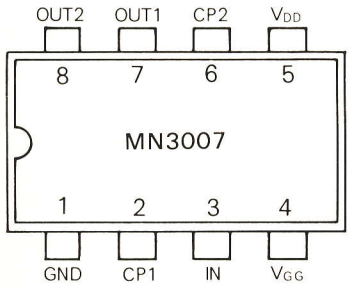
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			700	pF
Clock Frequency	f_{CP}	10		100	kHz
Clock Pulse Width *2	t_{cpw}			0.5T*1	
Clock Rise Time *2	t_{cpr}			500	nsec
Clock Fall Time *2	t_{cpf}			500	nsec
Clock Cross Point	Vx	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25°C, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

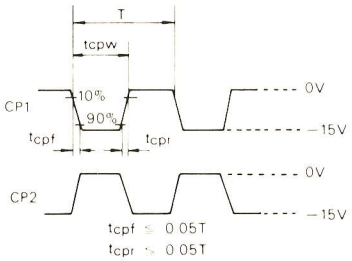
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		5.12		51.2	msec
Input Signal Frequency	f_i	f_{CP}=40kHz, V_i=1.5Vrms, 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i=1kHz, THD=2.5%			1.5	Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i=1kHz, V_i=1.5Vrms	−4	0	4	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.5	2.5	%
Noise Voltage	Vno	f_{CP}=100kHz Weighted by "A" curve			0.30	mVrms
Signal to Noise Ratio	S/N			80		dB

Terminal Assignments

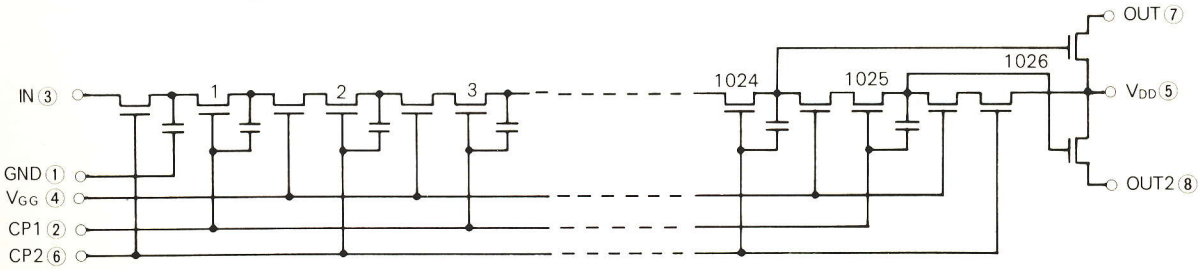


(Top View)

Clock Pulse Waveforms

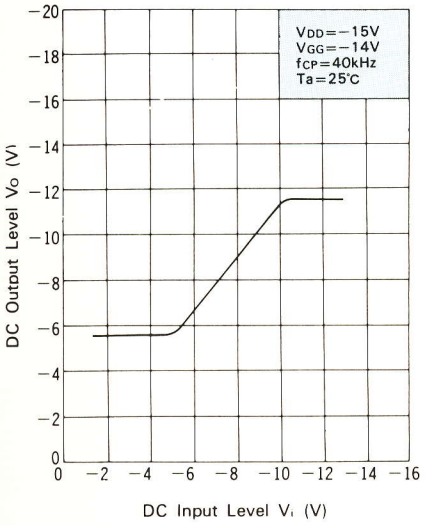


Circuit Diagram

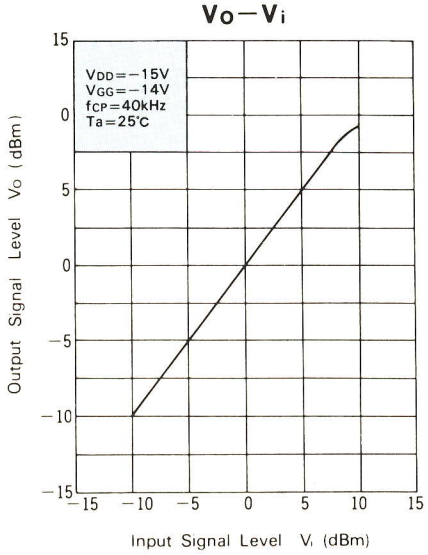


Typical Electrical Characteristic Curves

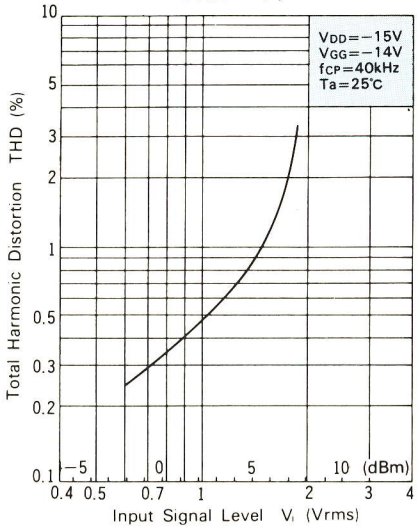
Vo—VI



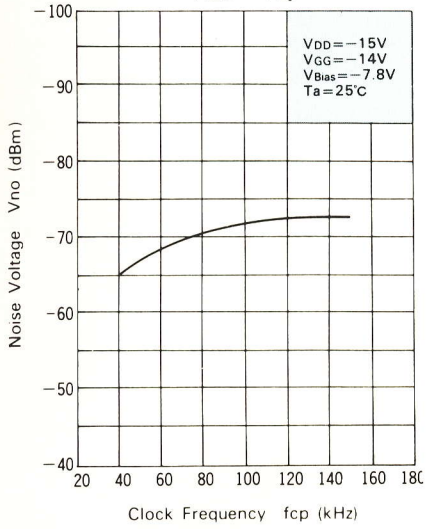
Vo—Vi



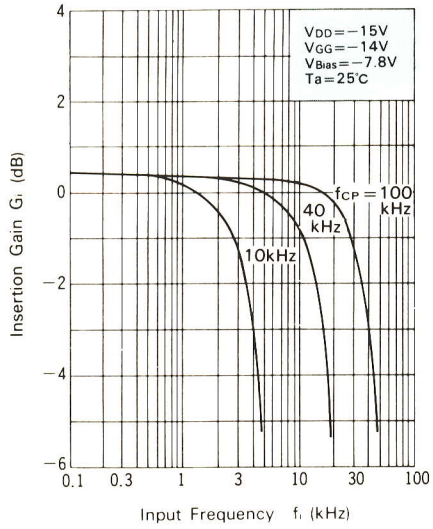
THD—Vi



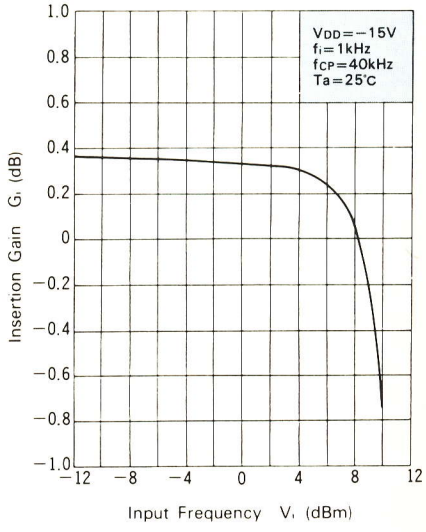
Vno—fcp



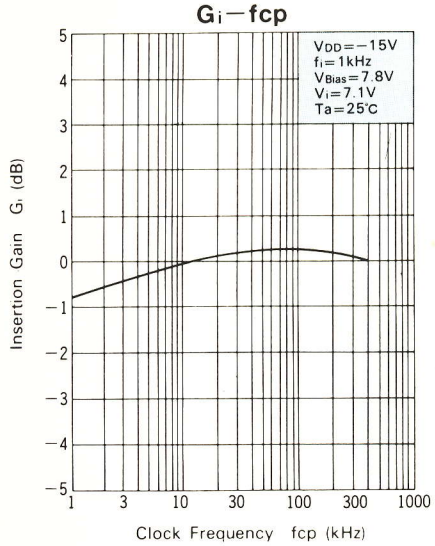
Gi—fi



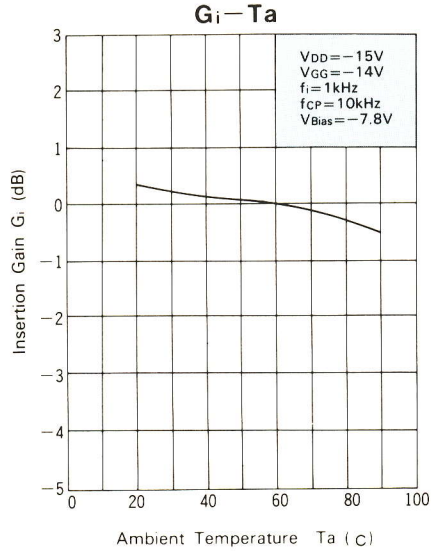
Gi—Vi



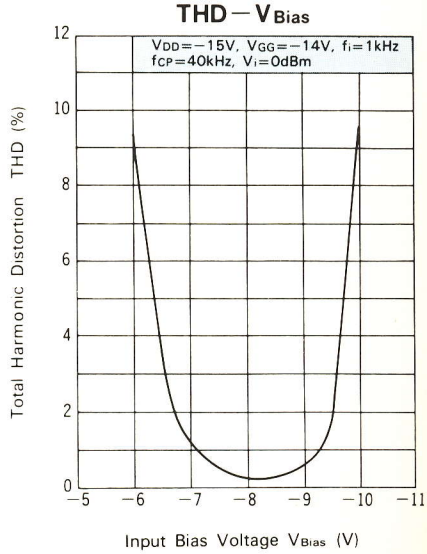
Gi—fcp



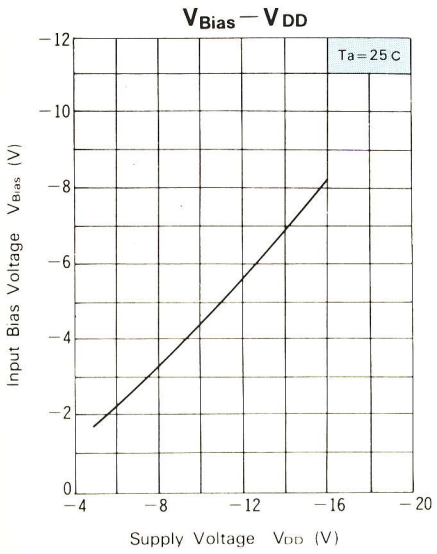
Gi—Ta

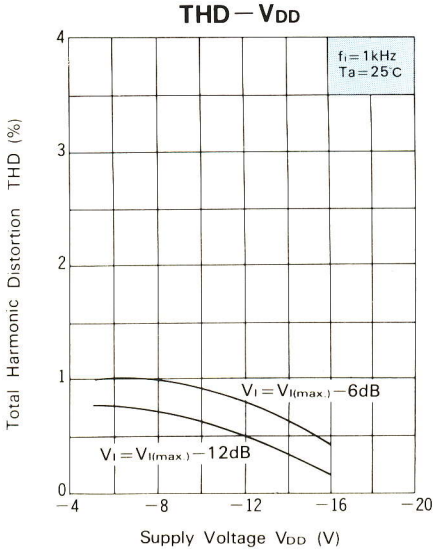


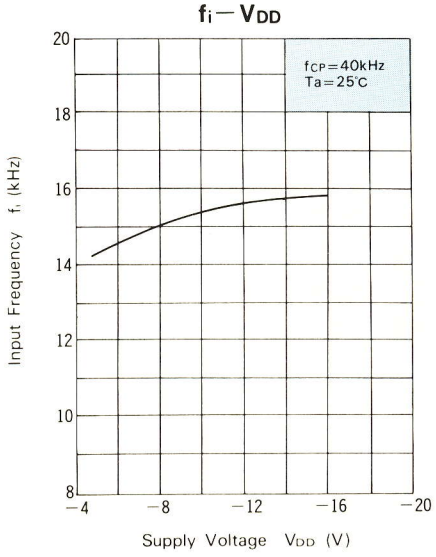
THD—VBias

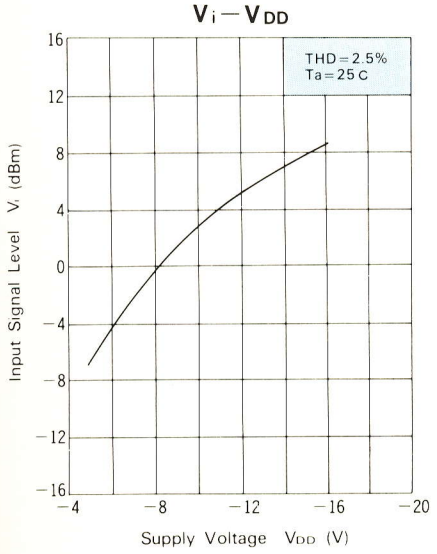


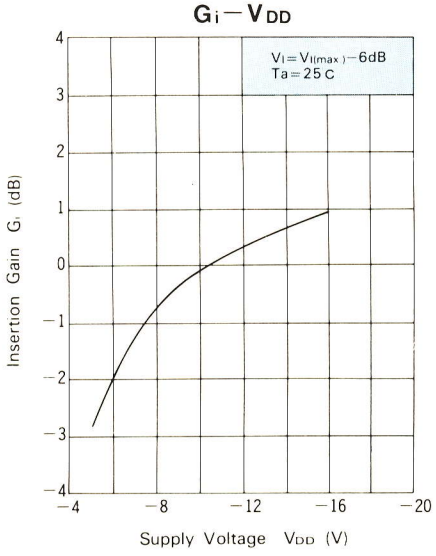
Supply Voltage Characteristics

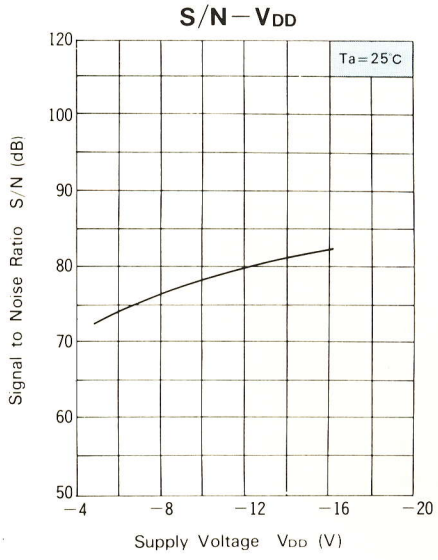




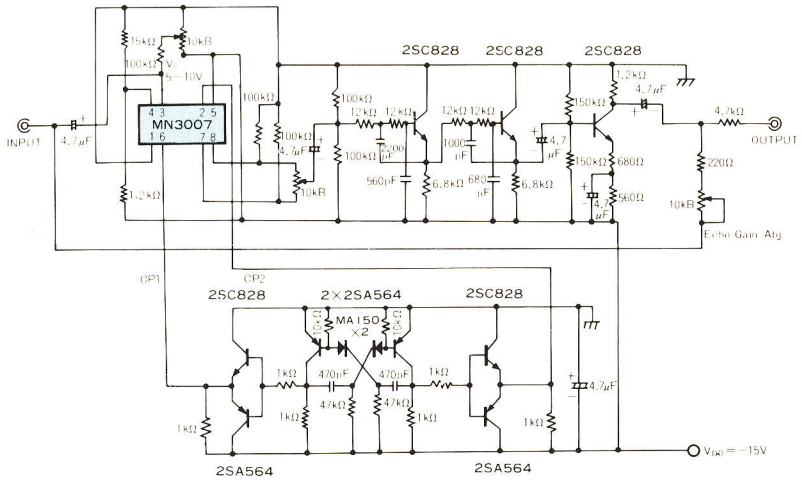








Application Circuit



Echo Effect Generation Circuit (Signal Delay Over 10msec.)

MN3008

2048-STAGE LOW NOISE BBD

General Description

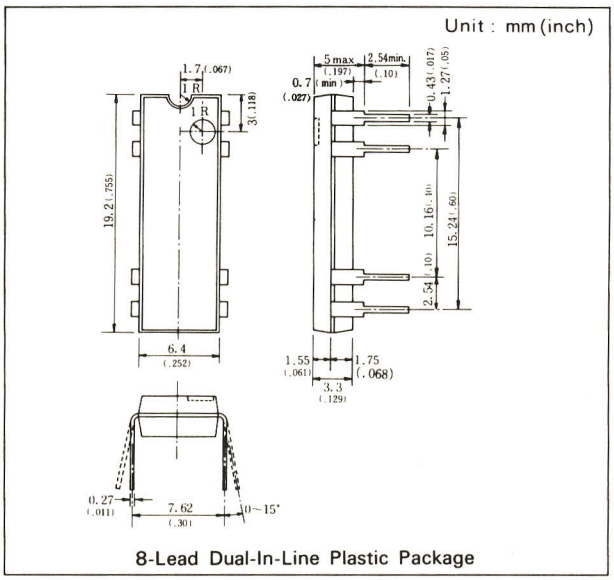
The MN3008 is a 2048-stage long delay BBD (Bucket Brigade Device) that provides a signal delay of up to 102.4msec. The MN3008 is particularly suitable for use as variable signal delay lines in audio frequency range.

Features:

- Wide range of variable delay time: 10.24～102.4msec.
- Clock component cancellation capability.
- No insertion loss: $L_i \simeq 0$ dB typ.
- Wide dynamic range: S/N ≃ 78dB typ.
- Wide frequency response: $f_i < 12$kHz.
- Total harmonic distortion: THD=0.5% typ. (V_i=0.78Vrms)
- Clock frequency range: 10～100kHz.
- P-channel silicon gate, tetrode MOS transistors configuration.
- 8-lead dual-in-line plastic package.

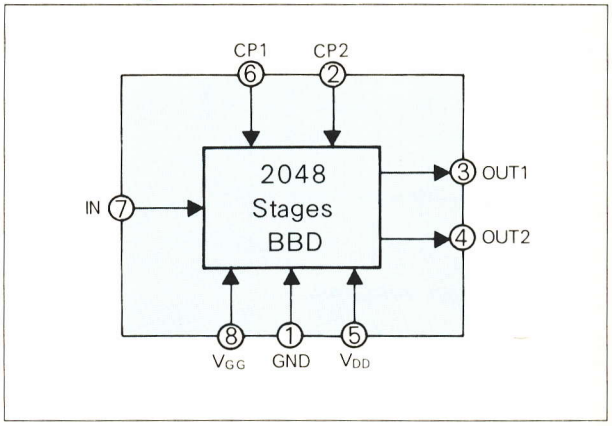
Applications:

- Reverberation effect of echo microphones and stereo equipment.
- Chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.



8-Lead Dual-In-Line Plastic Package

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	10.24～102.4	msec
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	78	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18～+0.3	V
Output Voltage	V_O	−18～+0.3	V
Operating Temperature	Topr	−20～+60	°C
Storage Temperature	Tstg	−55～+125	°C

Operating Conditions (Ta=25°C)

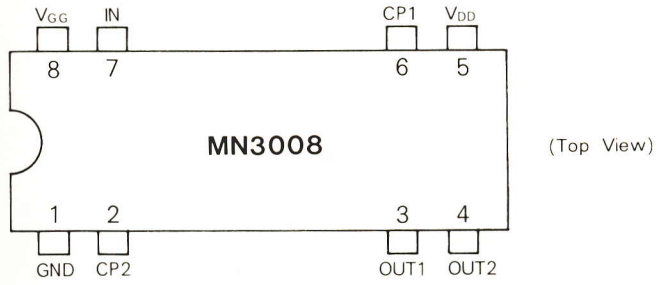
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			1400	pF
Clock Frequency	f_{CP}	10		100	kHz
Clock Pulse Width *2	t_{cpw}			0.5T*1	
Clock Rise Time *2	t_{cpr}			500	nsec
Clock Fall Time *2	t_{cpf}			500	nsec
Clock Cross Point	Vx	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25°C, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

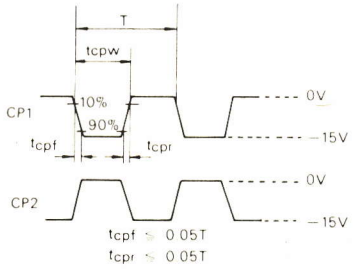
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		10.24		102.4	msec
Input Signal Frequency	f_i	f_{cp}=40kHz, V_i=1.3Vrms. 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{cp}=40kHz, f_i=1kHz, THD=2.5%			1.5	Vrms
Insertion Loss	L_i	f_{cp}=40kHz, f_i=1kHz, V_i=1.3Vrms		0		dB
Total Harmonic Distortion	THD	f_{cp}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.5		%
Noise	Vno	f_{cp}=100kHz Weighted by "A" curve			0.30	mVrms
Signal to Noise Ratio	S/N			78		dB

Terminal Assignments

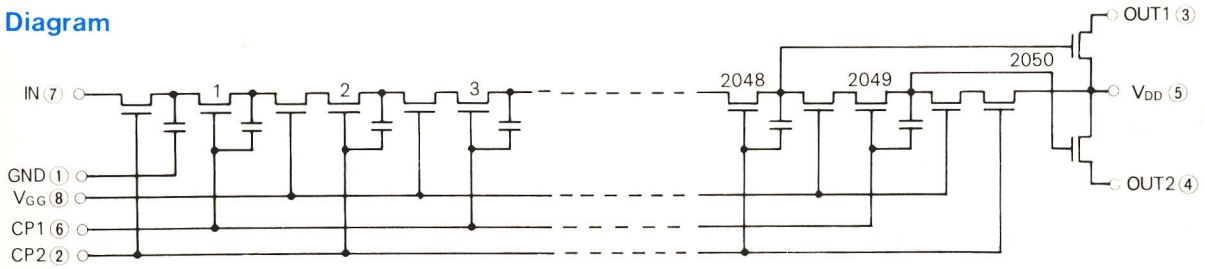


(Top View)

Clock Pulse Waveforms

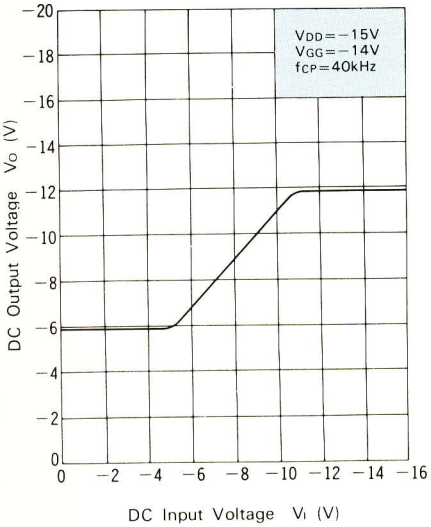


Circuit Diagram

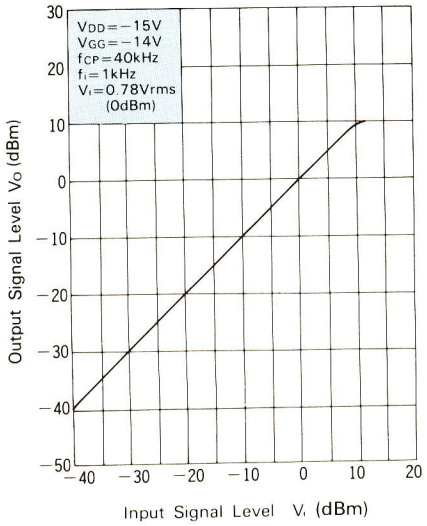


Typical Electrical Characteristic Curves

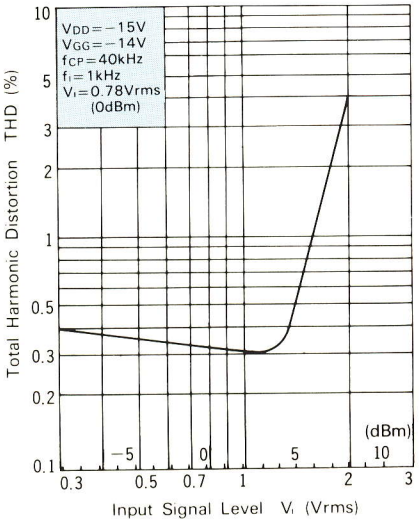
Vo−VI



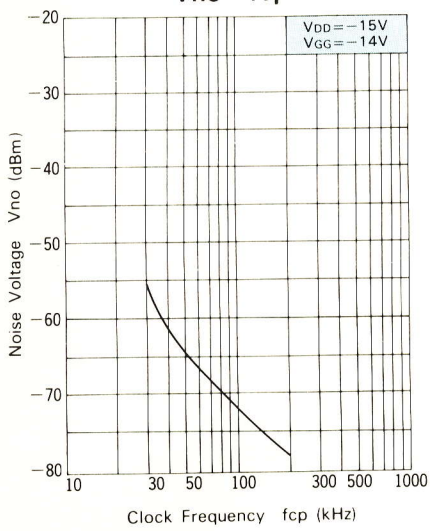
Vo−Vi



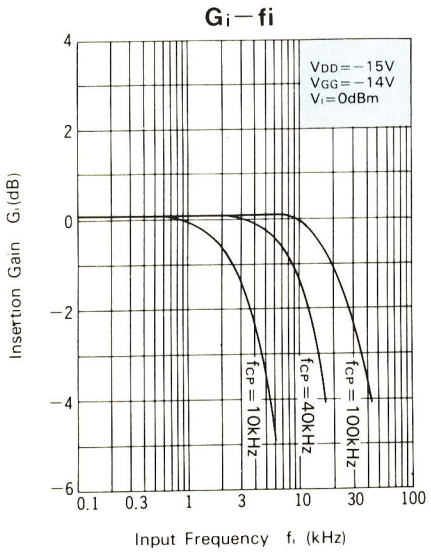
THD−Vi



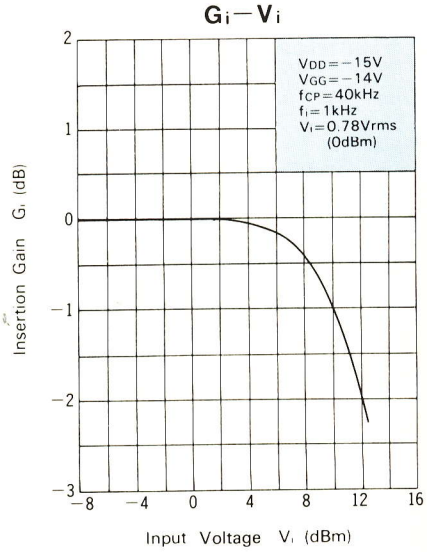
Vno−fcp



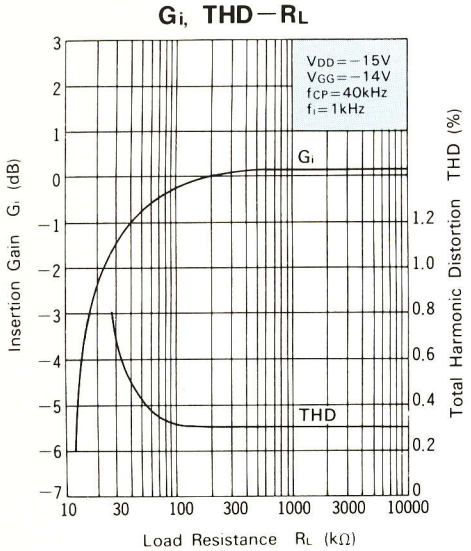
Gi−fi



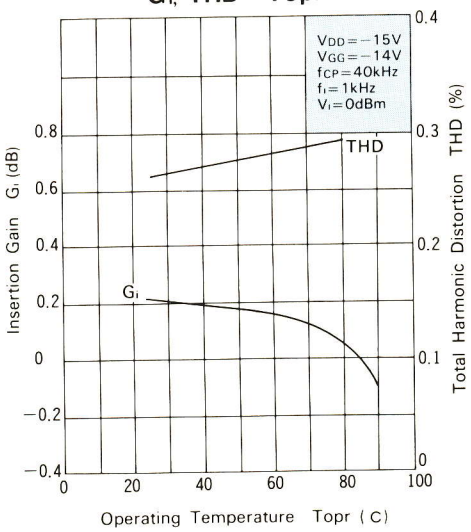
Gi−Vi



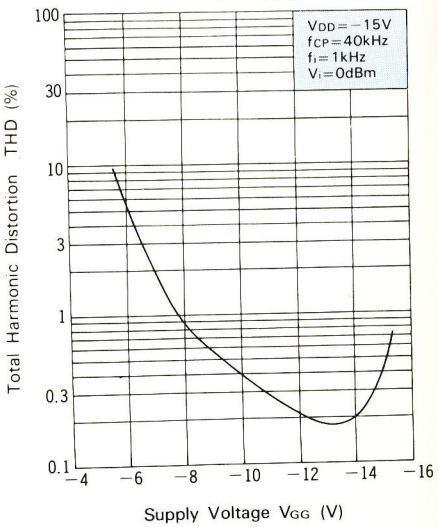
Gi, THD−RL



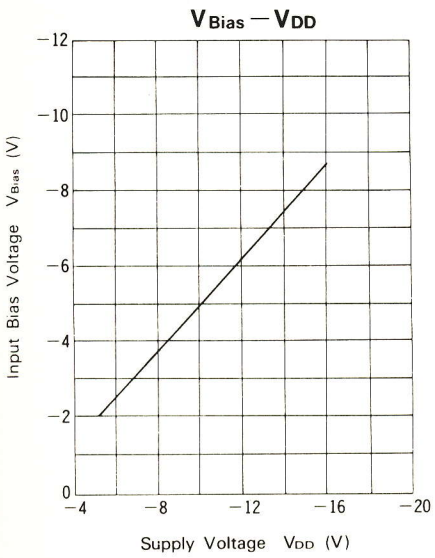
Gi, THD−Topr

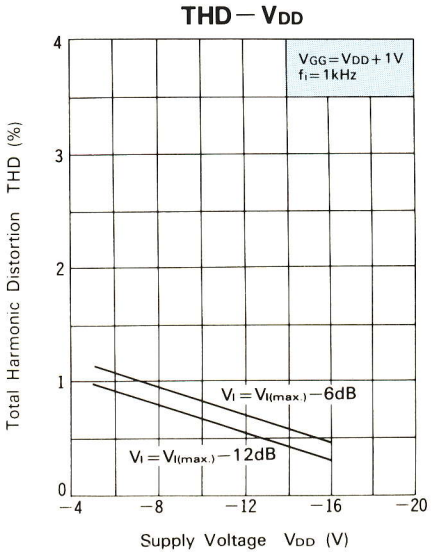


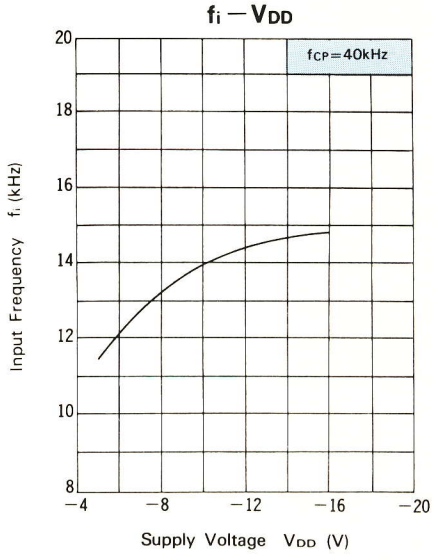
THD−VGG

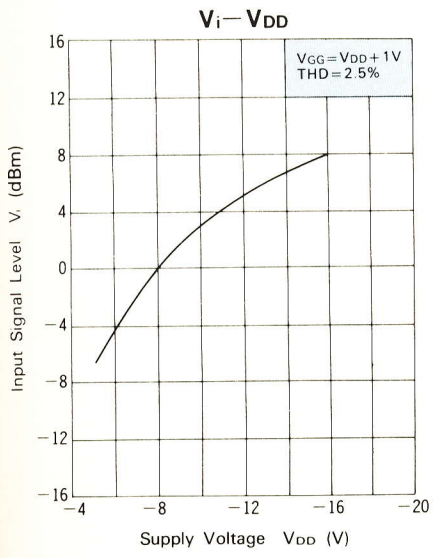


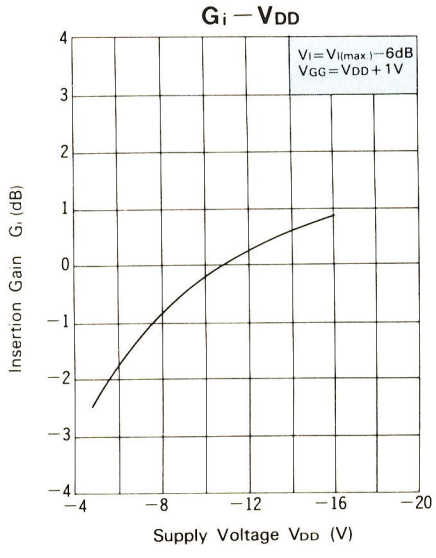
Supply Voltage Characteristics

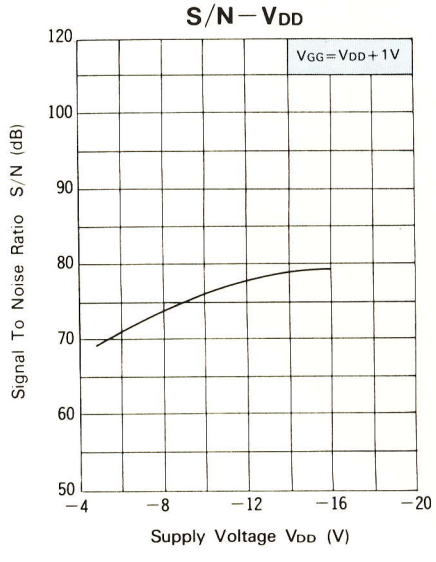




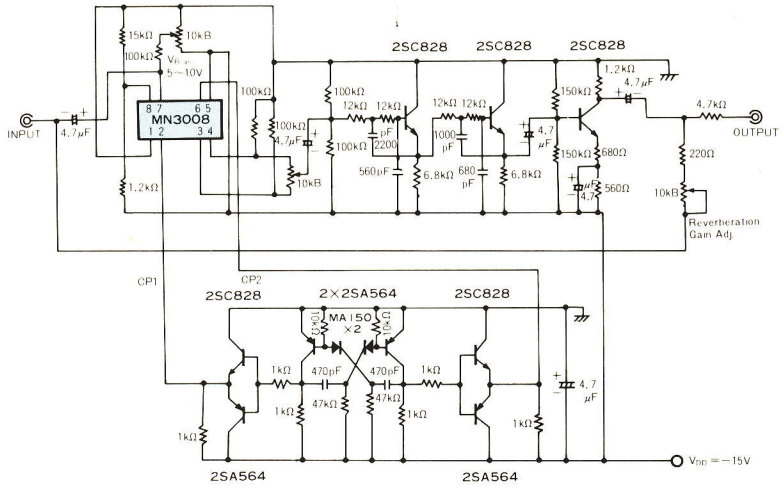








Application Circuit



Reverberation Effect Generation Circuit (Signal Delay Over 100msec.)

MN3009

256-STAGE LOW NOISE BBD

General Description

The 3009 is a 256-stage BBD (Bucket Brigade Device) having a wide dynamic range and low distortion characteristics. The 3009 provides a signal delay of up to 12.8msec and is particularly suitable as a device for generation of vibrato and / or chorus effects in electronic musical instruments.

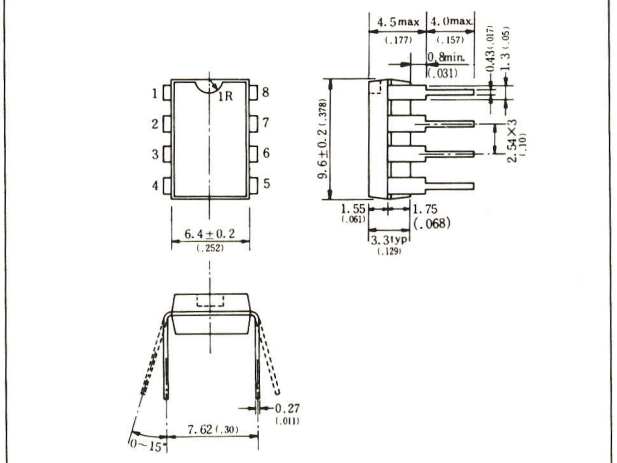
Features:

- Variable delay time: 0.64~12.8msec.
- Clock component cancellation capability.
- Low insertion loss: $L_i \simeq 0$ dB typ.
- Wide dynamic range: S/N ≃ 88dB typ.
- Wide frequency response: $f_i < 14$kHz.
- Total harmonic distortion: THD=0.3% typ. (V_i=0.78Vrms)
- Clock frequency range: 10~200kHz.
- P-channel silicon gate, tetrode MOS transistors configuration.
- 8-lead dual-in-line plastic package.

Applications:

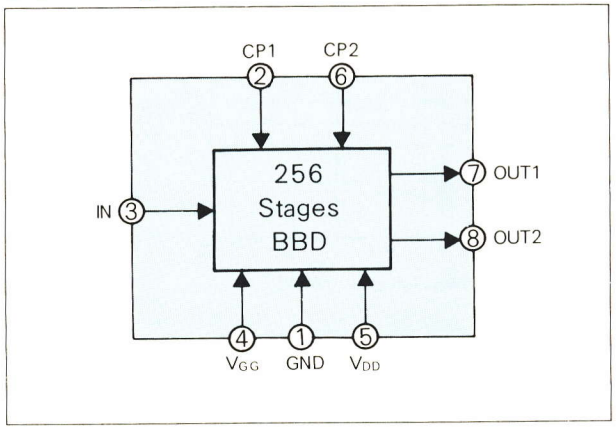
- Vibrato and / or chorus effects in electronic organs and musical instruments.
- Variable or fixed delay of analog signals.

Unit : mm (inch)



8-Lead Dual-In-Line Plastic Package

Block Diagram



Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	0.64~12.8	msec
Total Harmonic Distortion	THD	0.3	%
Signal to Noise Ratio	S/N	88	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18~+0.3	V
Output Voltage	V_O	−18~+0.3	V
Operating Temperature	Topr	−20~+60	°C
Storage	Tstg	−55~+125	°C

Operating Conditions (Ta=25°C)

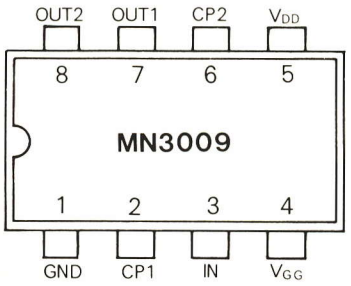
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			200	pF
Clock Frequency	f_{CP}	10		200	kHz
Clock Pulse Width *2	t_{cpw}			0.5T *1	
Clock Rise Time *2	t_{cpr}			500	nsec
Clock Fall Time *2	t_{cpf}			500	nsec
Clock Cross Point	Vx	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25°C, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

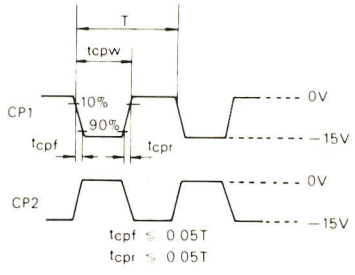
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		0.64		12.8	msec
Input Signal Frequency	f_i	f_{CP}=40kHz, V_i=1.8Vrms 3dB down (0dB at f_i=1kHz)			14	kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i=1kHz, THD=2.5%			1.7	Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i=1kHz, V_i=1.8Vrms		0		dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.3		%
Noise	Vno	f_{CP}=100kHz Weighted by "A" curve			150	μVrms
Signal to Noise Ratio	S/N	Maximum output voltage to noise voltage		88		dB

Terminal Assignments

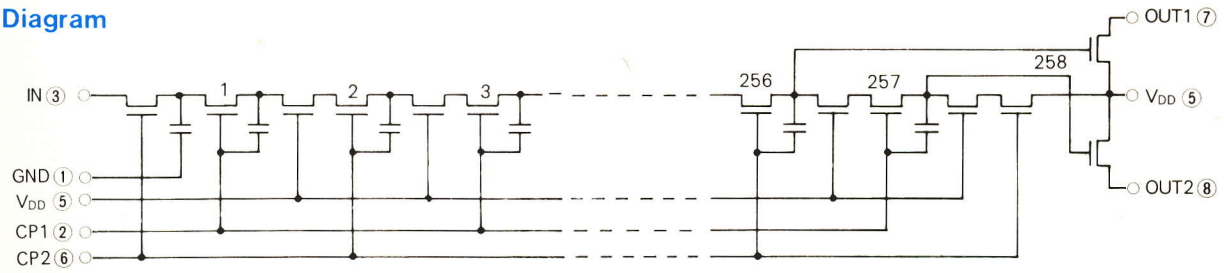


(Top View)

Clock Pulse Waveforms

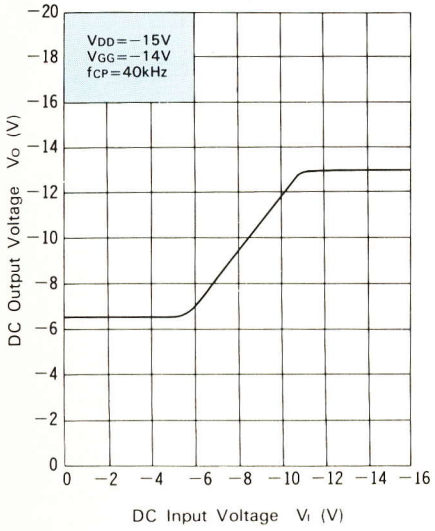


Circuit Diagram

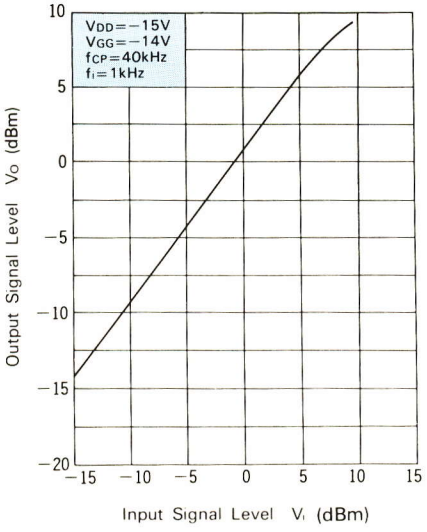


Typical Electrical Characteristic Curves

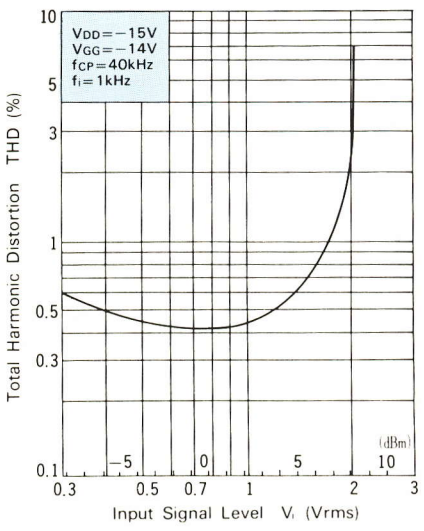
$V_O - V_I$



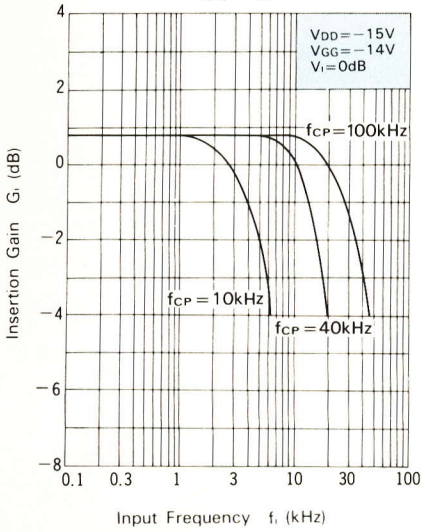
$V_O - V_i$



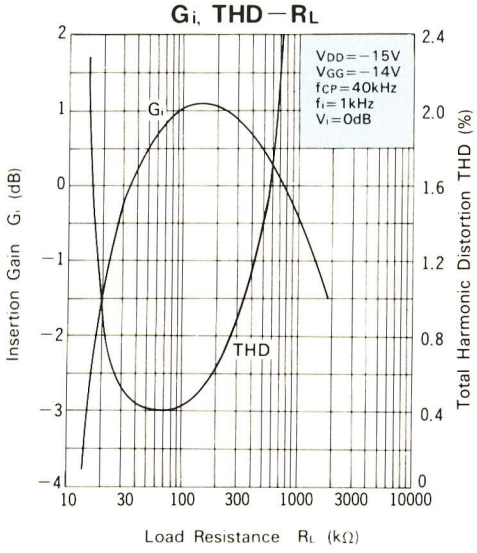
$THD - V_i$



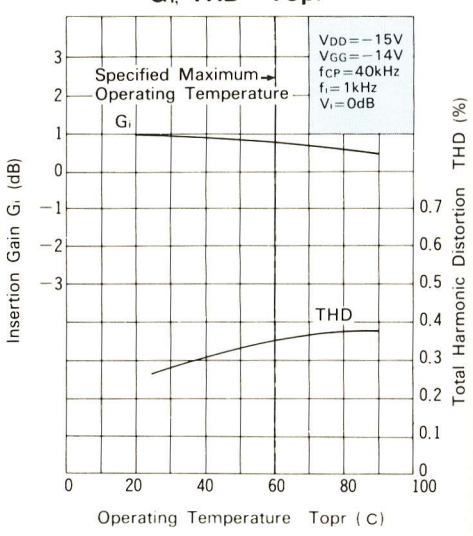
$G_i - f_i$



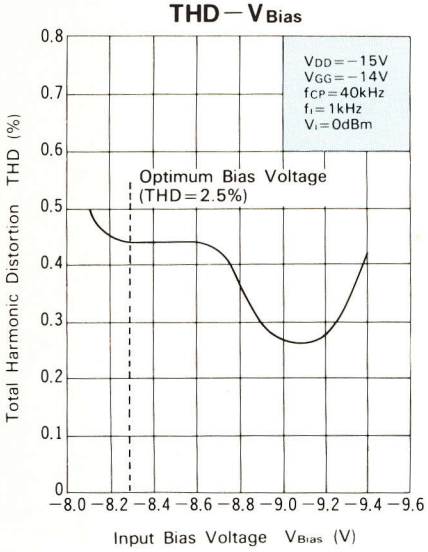
G_i, $THD - R_L$



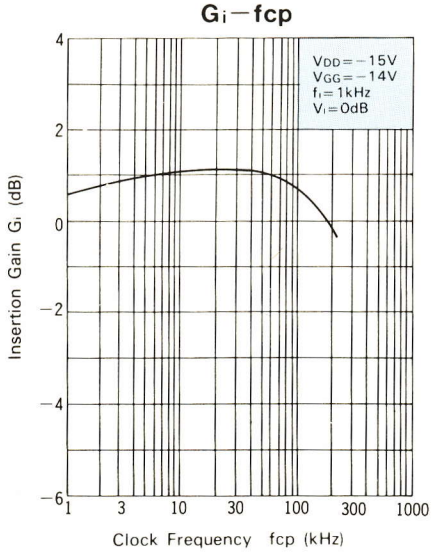
G_i, $THD - T_{opr}$



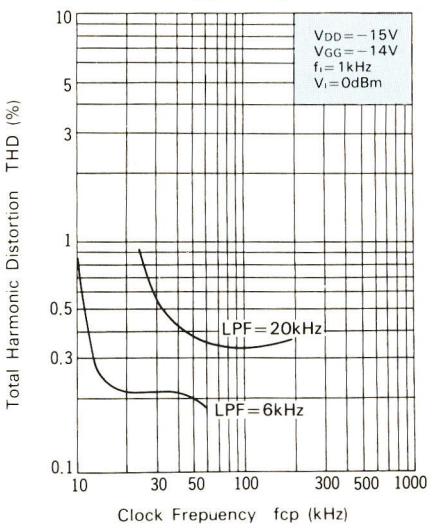
$THD - V_{Bias}$



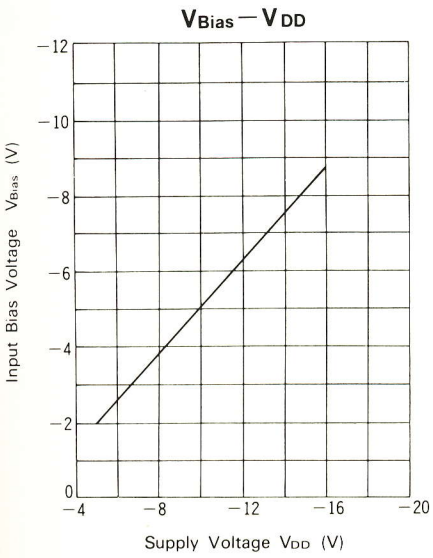
$G_i - f_{cp}$

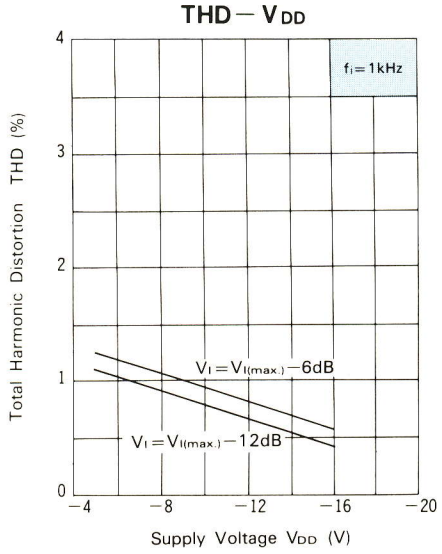


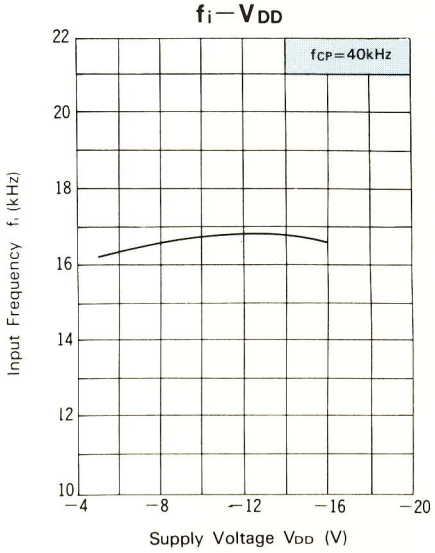
$THD - f_{cp}$

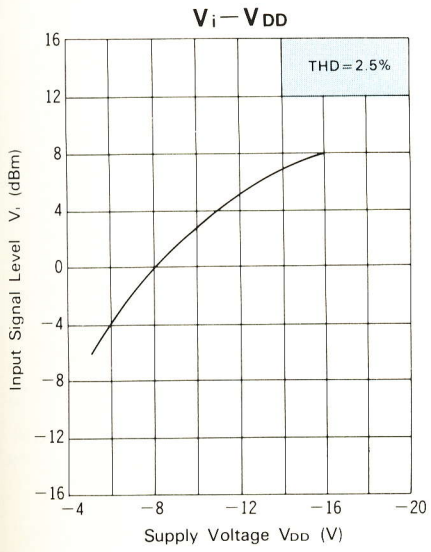


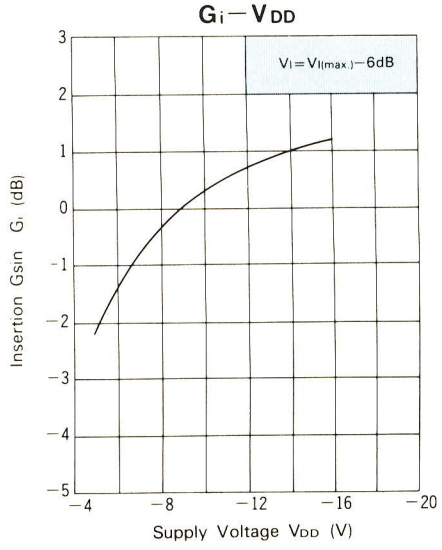
Supply Voltage Characteristics

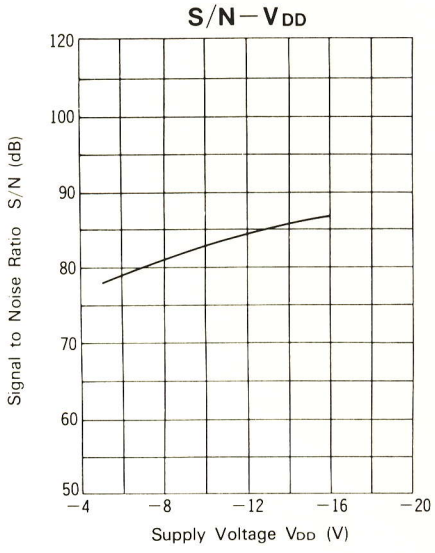




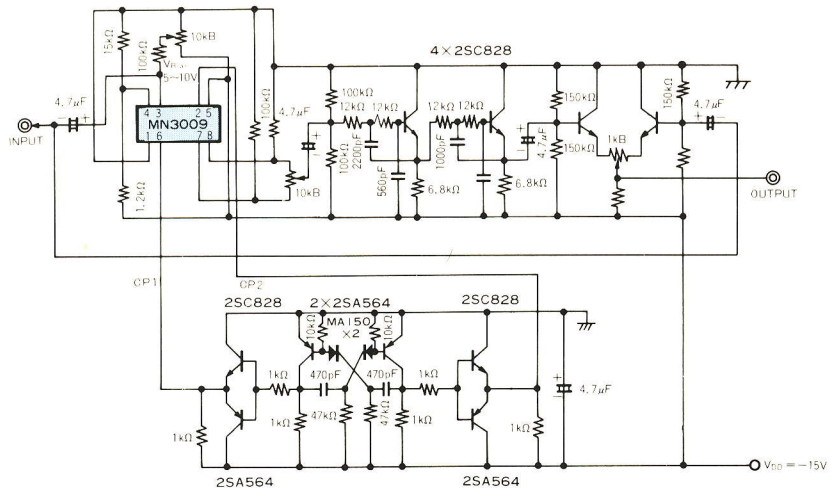








Application Circuit



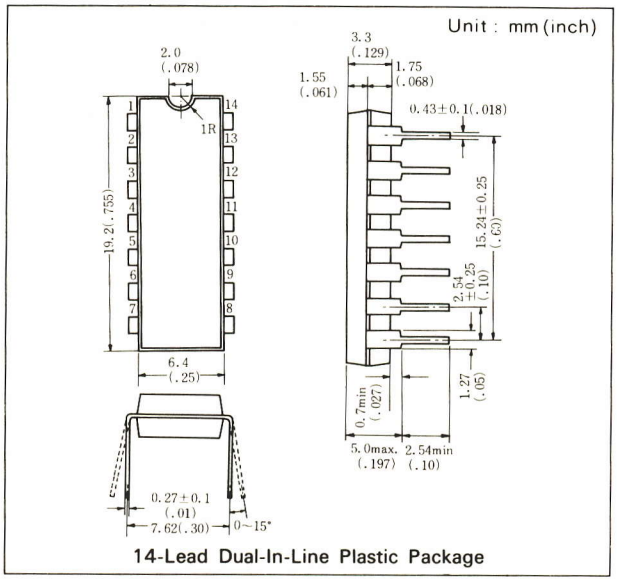
Chorus Effect Generation Circuit

MN3010

DUAL 512-STAGE LOW NOISE BBD

General Description

The MN3010 is a dual 512-stage low noise BBD having a wide dynamic range and low distortion characteristics. The device contains two identical BBD's on a single chip with independent input, output and clock terminals as well as common power supply terminals. Each 512-stage BBD provides a signal delay of up to 25.6msec. The two identical BBD's on a same chip offer uniform characteristics and space saving advantage when they are used in parallel or series connection.

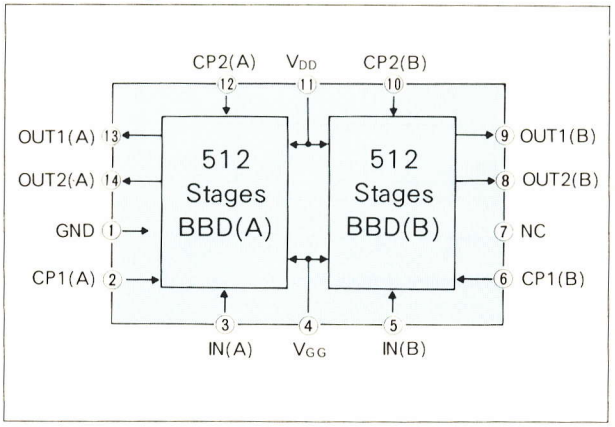


14-Lead Dual-In-Line Plastic Package

Features:

- **Wide range of variable delay time:**
  2.56~25.6msec. (512-stage)
  5.12~51.2msec. (512×2-stage)
- **Clock component cancellation capability.**
- **No insertion loss: $L_i \simeq 0$ dB typ.**
- **Wide dynamic range: S/N ≃ 85dB typ.**
- **Wide frequency response: f_i < 12kHz.**
- **Total harmonic distortion: THD=0.4% typ. (V_i=0.78Vrms)**
- **Clock frequency range: 10~100kHz.**
- **Dual 512-stage configuration: 1024-stage in series connection, and twice as large output in parallel connection.**
- **P-channel silicon gate, tetrode MOS transistors configuration.**
- **14-lead dual-in-line package.**

Block Diagram



Applications:

- **Vibrato and/ or chorus effects in electronic organs and musical instruments.**
- **Reverberation effect of electronic musical instruments.**
- **Variadle or fixed delay of analog signals.**

Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD} V_{GG}	−15, V_{DD} +1	V
Signal Delay Time	t_D	2.56~51.2	msec
Total Harmonic Distortion	THD	0.4	%
Signal to Noise Ratio	S/N	85	dB

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18 ~ +0.3	V
Output Voltage	V_O	−18 ~ +0.3	V
Operating Temperature	Topr	−20 ~ +60	°C
Storage Temperature	Tstg	−55 ~ +125	°C

Operating Conditions (Ta=25°C)

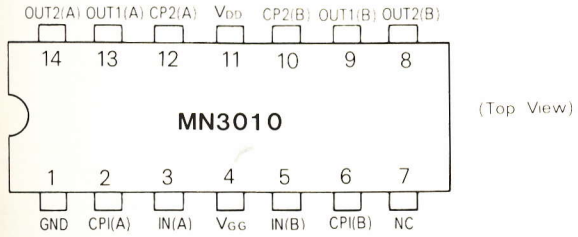
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			350	pF
Clock Frequency	f_{CP}	10		100	kHz
Clock Pulse Width *2	t_{cpw}			0.5T*1	
Clock Rise Time *2	t_{cpr}			500	nsec
Clock Fall Time *2	t_{cpf}			500	nsec
Clock Cross Point	Vx	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25°C, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

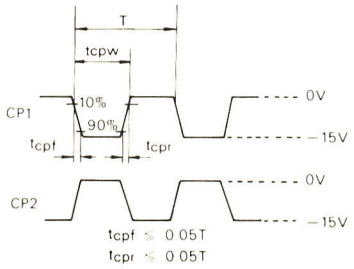
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		2.56		25.6	msec
Input Signal Frequency	f_i	f_{cp}=40kHz, V_i=1.8 Vrms, 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{cp}=40kHz, f_i=1kHz, THD=2.5%			1.8	Vrms
Insertion Loss	L_i	f_{cp}=40kHz, f_i=1kHz, V_i=1.8 Vrms		0		dB
Total Harmonic Distortion	THD	f_{cp}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.4		%
Noise Voltage	Vno	f_{cp}=100kHz Weighted by "A" curve			0.21	mVrms
Signal to Noise Ratio	S/N	Maximum output voltage to noise voltage		85		dB

Terminal Assignments

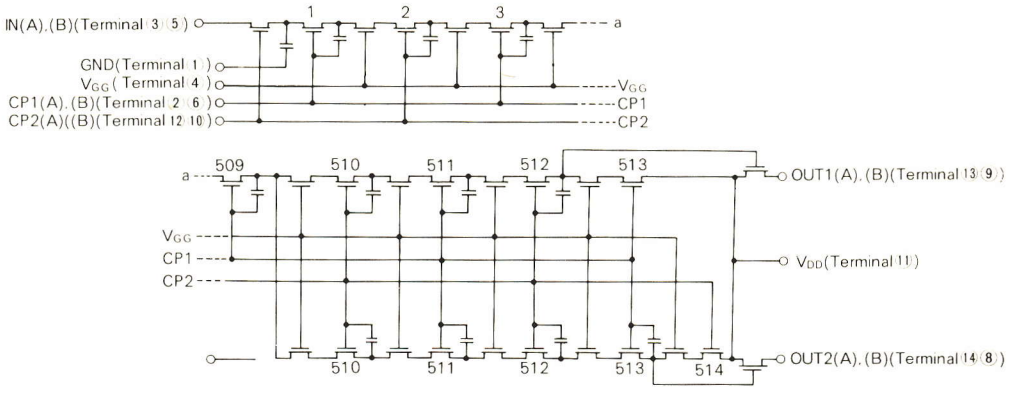


(Top View)

Clock Pulse Waveforms

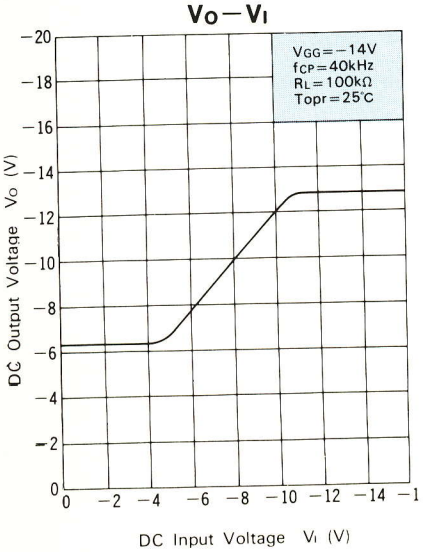


Circuit Diagram

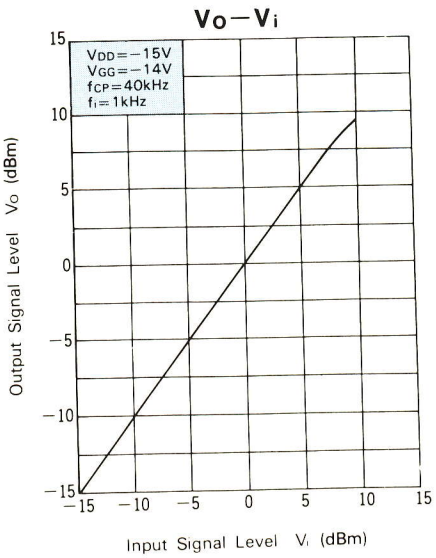


Typical Electrical Characteristic Curves

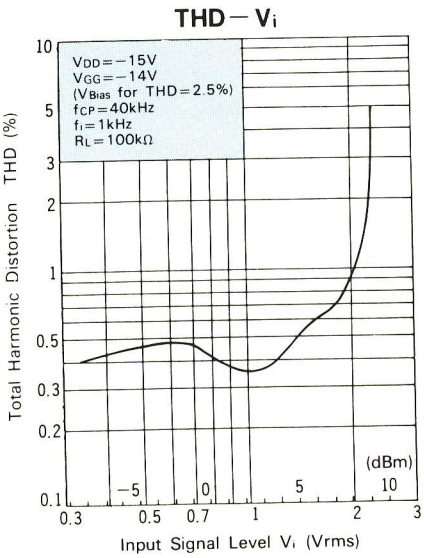
$V_O - V_I$



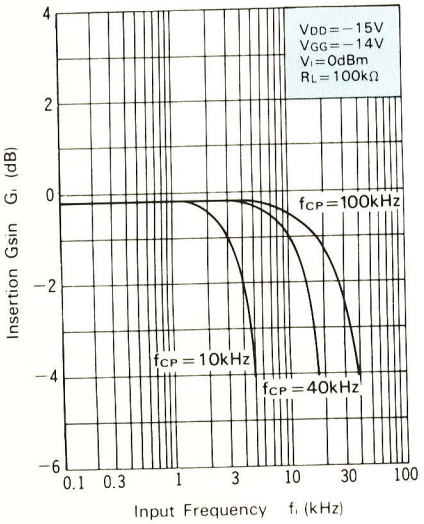
$V_O - V_i$



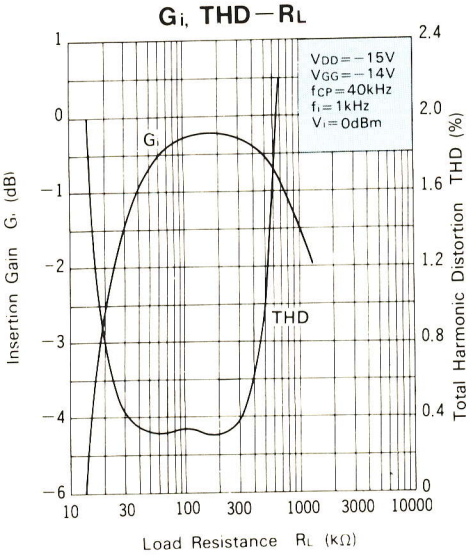
$THD - V_i$



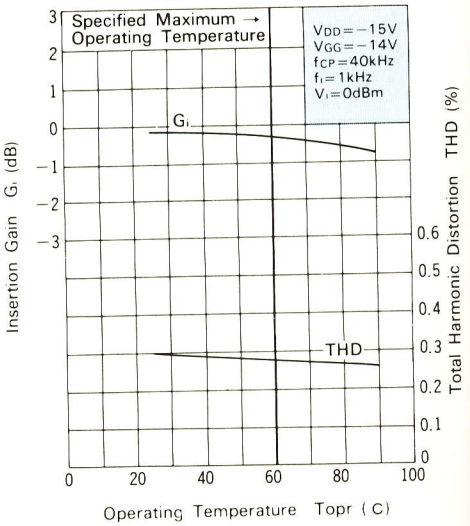
$G_i - f_i$



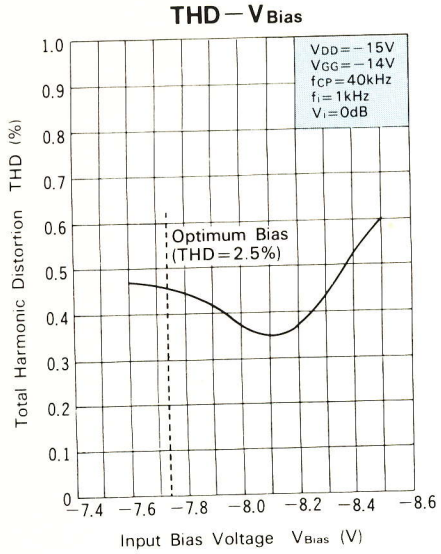
G_i, $THD - R_L$



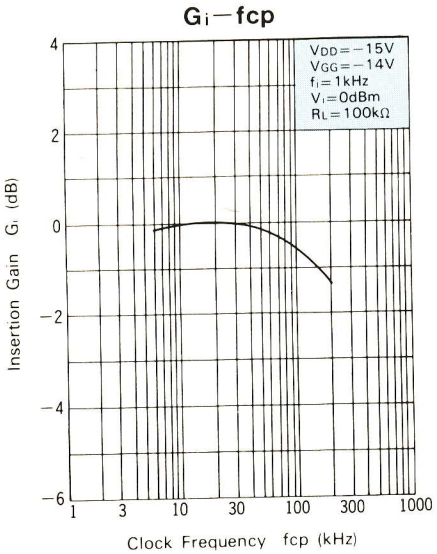
G_i, $THD - Topr$



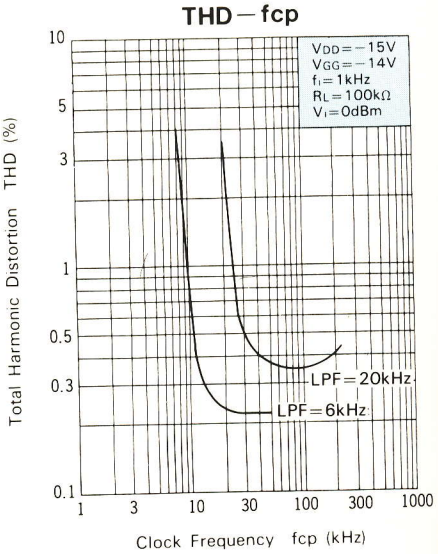
$THD - V_{Bias}$



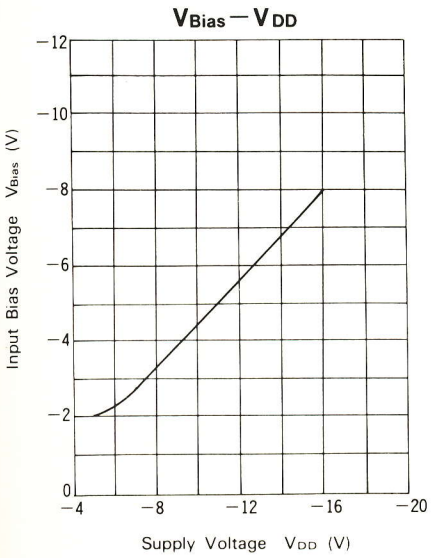
$G_i - fcp$

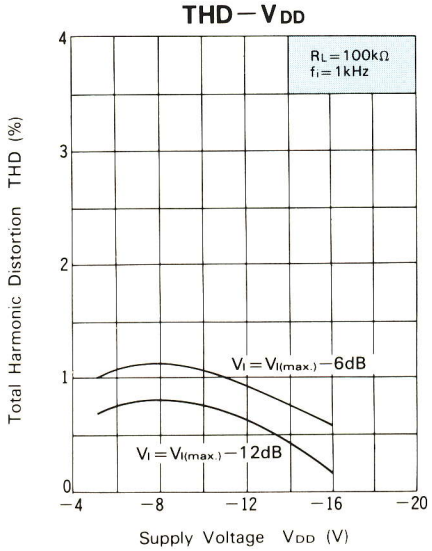


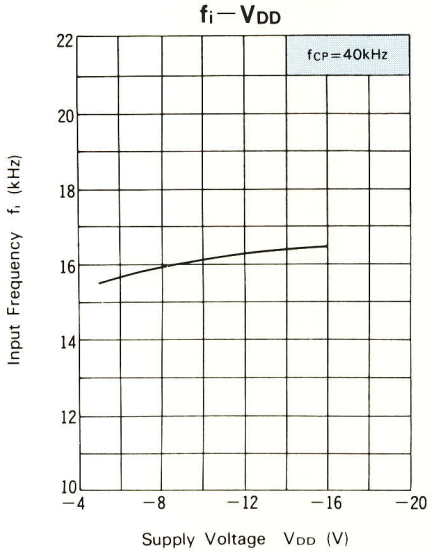
$THD - fcp$

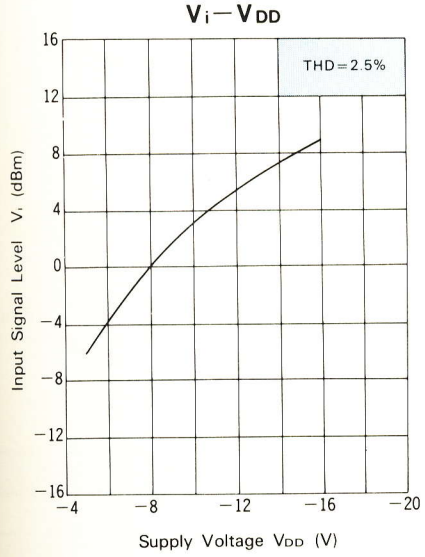


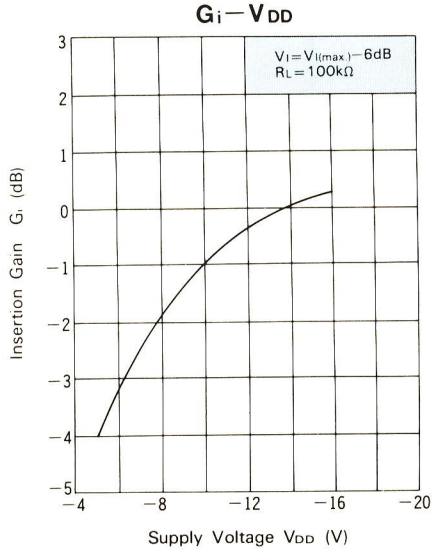
Supply Voltage Characteristics

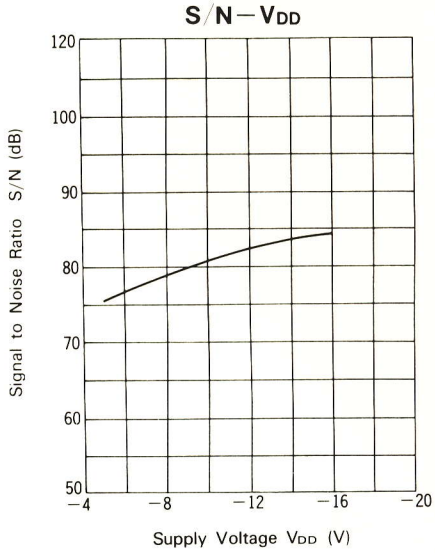




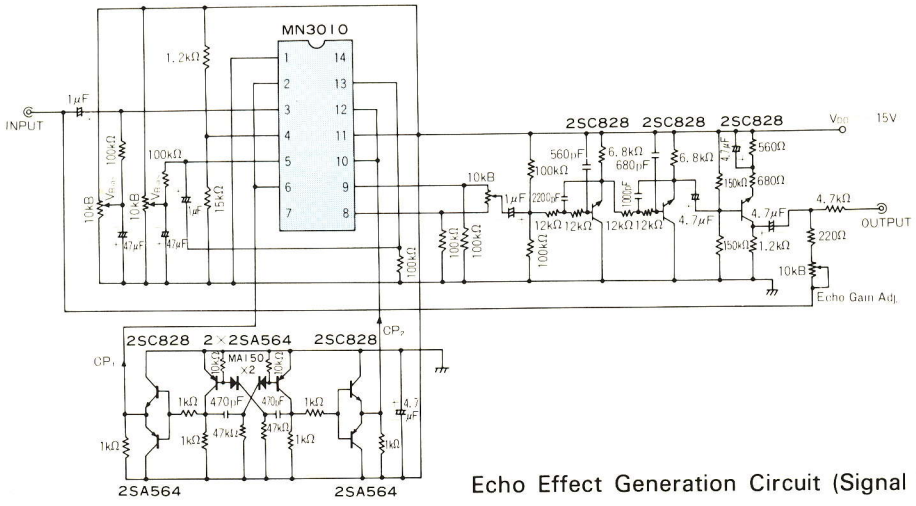








Application Circuit



Echo Effect Generation Circuit (Signal Delay Over 10msec.)

MN3011

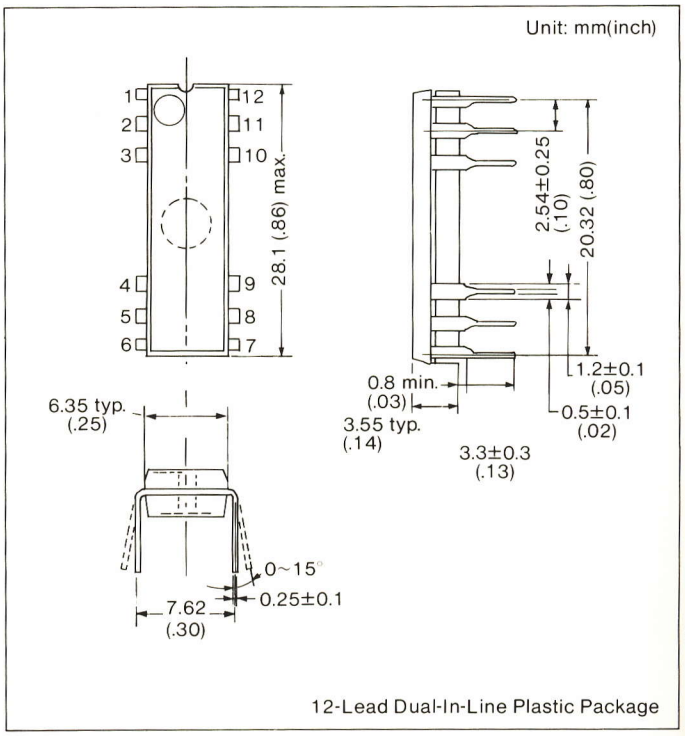
3328 - Stage Multi-Tap BBD (MN3011) for Audio Signal Delays

General Description

The MN3011 is a 3328-stage low noise BBD (Bucket Brigade Device) designed to provide simultaneously six different delay outputs with respect to a signal input. A proper mixing of the six differently delayed signals generates highly effective reverberation. The delay times can be varied by the clock frequency control.

Features

- **3328-stage with 6 different output stages**
- **6 stages not in multiple proportion with each other so that a proper mixing of the six differently delayed output signals generates a highly effective reverberation.**
- **Clock component cancellation capability.**
- **Wide dynamic range: S/N ≥ 76 dB typ.**
- **No insertion loss: Li = 0 dB typ.**
- **Total harmonic distortion: THD = 0.4% typ.**
- **P-channel silicon gate, tetrode MOS transistors configuration**

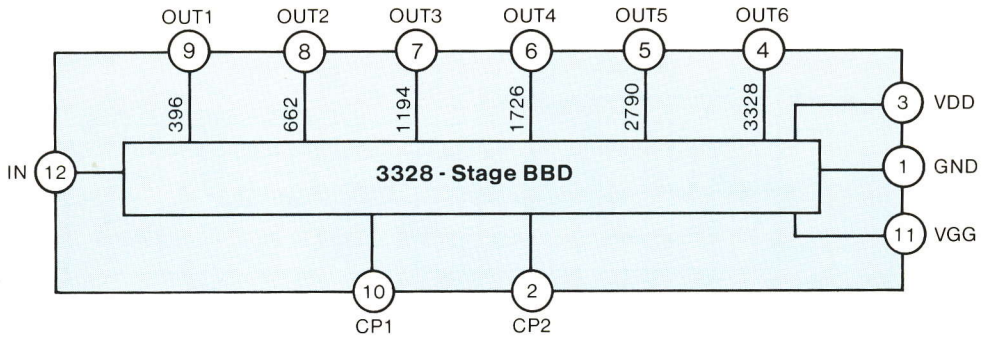


12-Lead Dual-In-Line Plastic Package

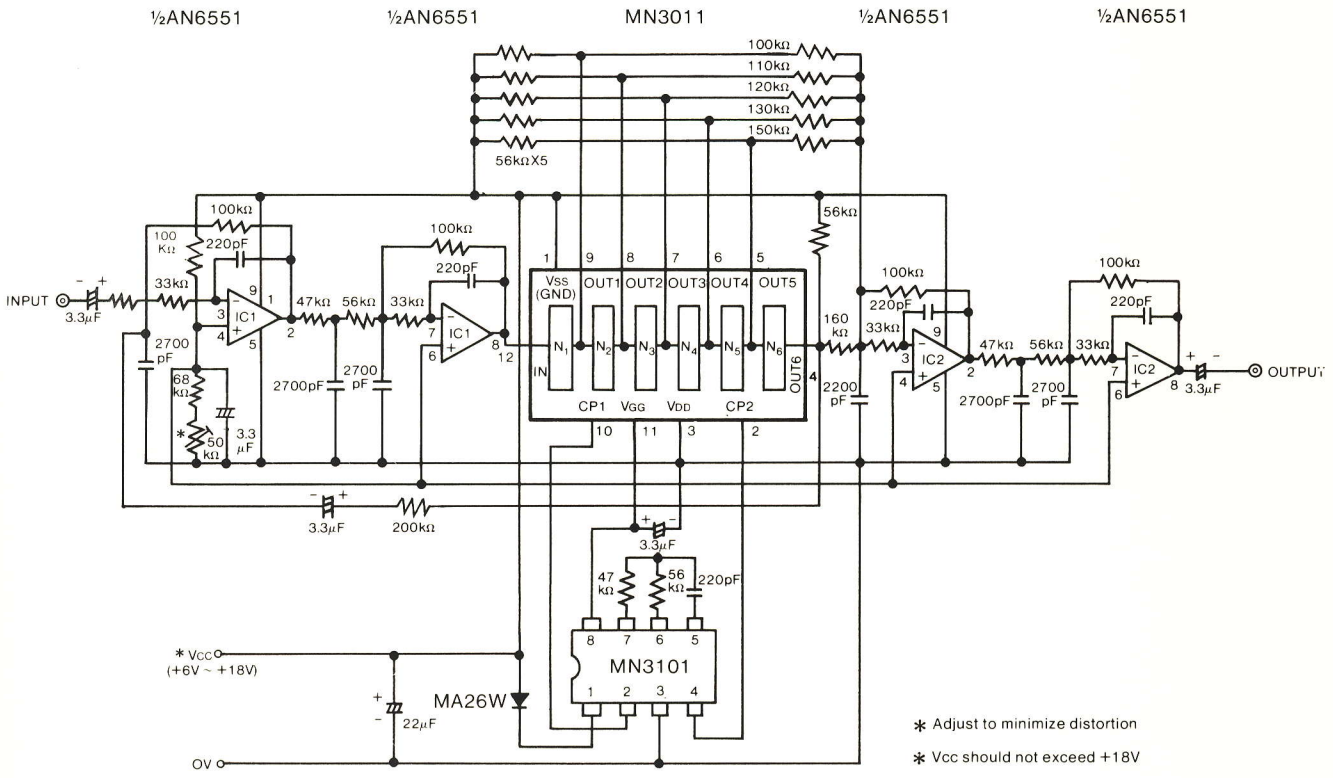
Maximum Delay Times for 6 Different Output Stages

Tapped Output Terminals	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	Remark
BBD stages (stages)	396	662	1194	1726	2790	3328	
Maximum Delay Time (msec.)	19.8	33.1	59.7	86.3	139.5	166.4	Clock 10KHz

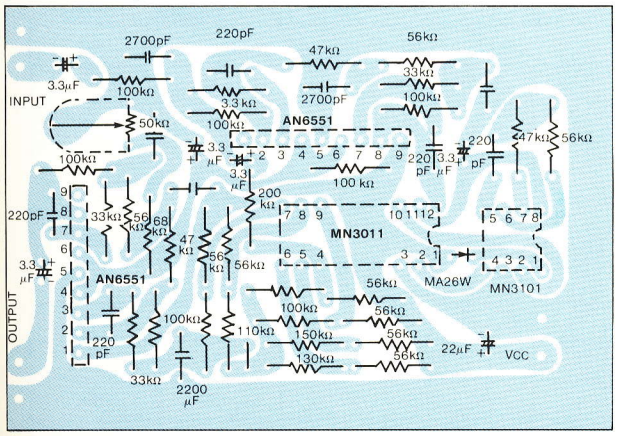
Block Diagram



Application Circuit – Reverberation Effect Generation Circuit



Printed Circuit Board Layout
(Actual Size)



Electrical Characteristics of The Application Circuit
(V_{CC} = +15V, Ta = 25°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply Current	I_{CC}			11(8)	15(10)	mA
Total Power Dissipation	Ptot			165 (70)		mW
Signal Delay Time	t_D	OUT6: f_{CP} = 15~20kHz	83	98	111	msec
Cutoff Frequency	f_{CO}			3		kHz
Input Signal Swing	V_i	THD = 2.5%			1.1(0.5)	Vrms
Insertion Loss	L_i	OUT3: f_i = 1kHz V_i = 300mV	0	2	4	dB
Total Harmonic Distortion	THD	f_i = 1kHz V_i V_i(max) -6dB		0.4 (0.5)		%
Output Noise Voltage	Vno	OUT3:V_i = 0V		0.4 (0.4)		mVrms
Signal to Noise Ratio	S/N	$V_S = V_i$(max)		70 (60)		dB

Note: Values in parenthesis for V_{CC} = +9V.

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_1	−18~+0.3	V
Output Voltage	VO	−18~+0.3	V
Operating Temperature	Topr	−20~+70	°C
Storage Temperature	Tstg	−55~+125	°C

Note: All voltages with respect to GND = 0V.

Operating Conditions (Ta = 25°C)

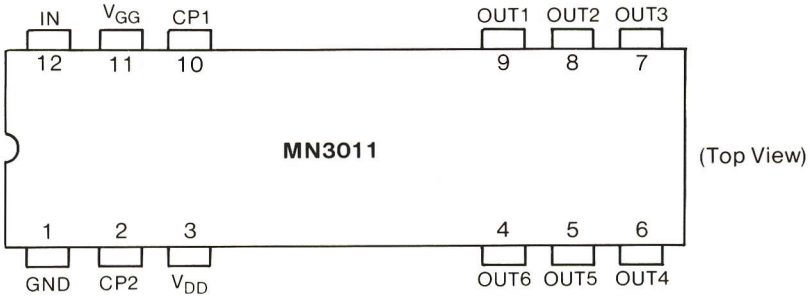
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	VDD	−14	−15	−16	V
Gate Supply Voltage	VGG		VDD + 1		V
Clock Voltage "H" Level	VCPH	0		−1.3	V
Clock Voltage "L" Level	VCPL		VDD		V
Clock Input Capacitance	CCP			2300	pF
Clock Frequency	fcp	10		100	kHz
Clock Pulse Width	tcpw			0.5T *	
Clock Rise Time	tcpr			500	nsec
Clock Fall Time	tcpf			500	nsec

*T = $1/f_{cp}$

Electrical Characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 56K\Omega$)

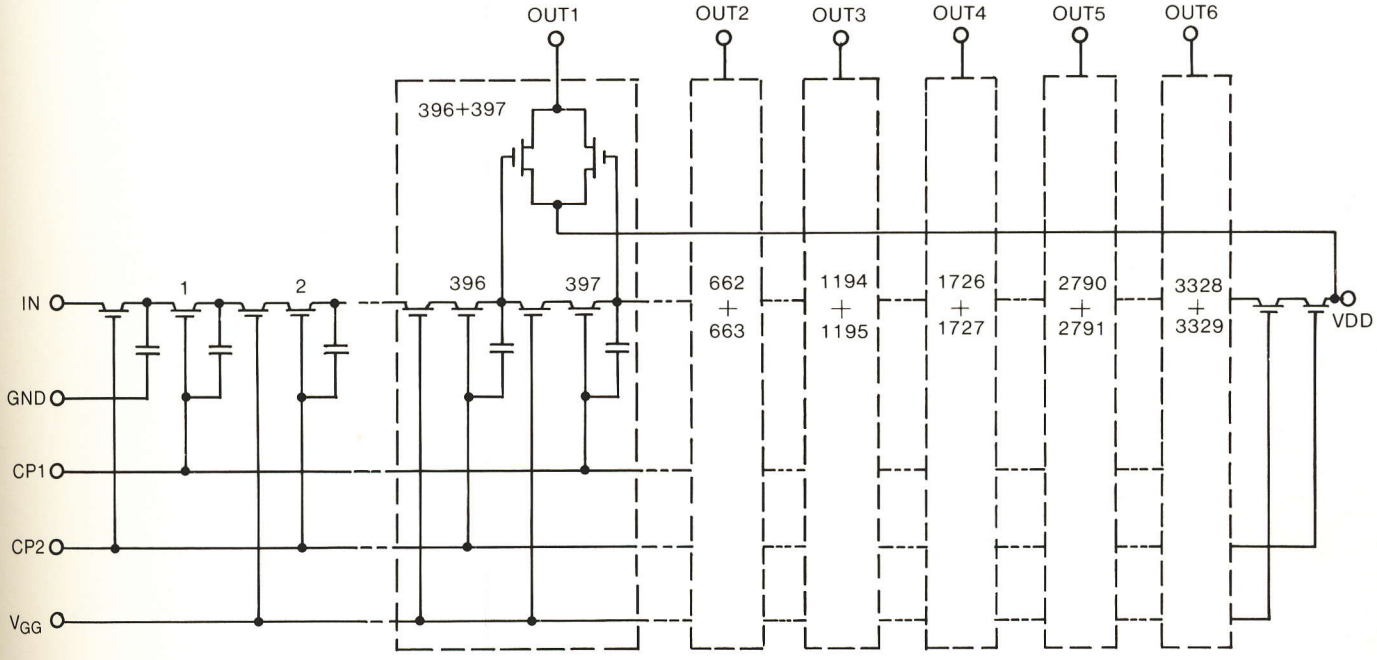
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time						
Terminal OUT1	tD1	fcp = 10kHz~100kHz	1.98		19.8	msec
Terminal OUT2	tD2		3.31		33.1	msec
Terminal OUT3	tD3		5.97		59.7	msec
Terminal OUT4	tD4		8.63		86.3	msec
Terminal OUT5	tD5		13.95		139.5	msec
Terminal OUT6	tD6		16.64		166.4	msec
Input Signal Frequency	fi	fcp = 40kHz − 3dB			11	kHz
Input Signal Swing	Vi	THD = 2.5%			1.1	Vrms
Insertion Loss	Li	fcp = 40kHz, fi = 1kHz,		0		dB
Total Harmonic Distortion	THD	fcp = 40kHz. fi = 1kHz. Vi = 0.78Vrms		0.4		%
Noise Level						
OUT1, OUT2, OUT3	Vno1	fcp = 100KHz Weighted by "A" curve			270	μVrms
OUT4, OUT5, OUT6	Vno2				400	μVrms
Signal to Noise Ratio						
OUT1, OUT2, OUT3	S/N1	fcp = 100kHz Weighted by "A" curve		80		dB
OUT4, OUT5, OUT6	S/N2	Maximum output voltage to noise voltage		76		dB

Terminal Assignments

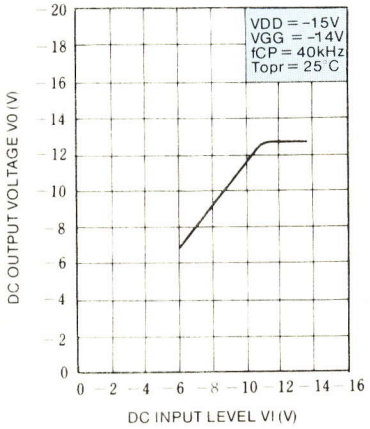


Pin No.	Symbol	Terminal	Functions
1	GND	Grounding	Ground connection
2	CP2	Clock Input 2	Fundamental clock pulse input for charge transfer
3	V_{DD}	V_{DD} Supply	−15V supply
4	OUT6	Output 6	3328th and 3329th stage synthetic output with clock component cancellation
5	OUT5	Output 5	2790th and 2791st stage synthetic output
6	OUT4	Output 4	1726th and 1727th stage synthetic output
7	OUT3	Output 3	1194th and 1195th stage synthetic output
8	OUT2	Output 2	662nd and 663rd stage synthetic output
9	OUT1	Output 1	396th and 397th stage synthetic output
10	CP1	Clock Input 1	Fundamental clock pulse input, inverted with respect to CP2
11	V_{GG}	V_{DD} Supply	V_{GG} bias supply input to each MOS transistor gate connected in series with BBD transfer gates $V_{GG} = V_{DD} + 1$
12	IN	Signal Input	Analog signal input The optimum DC bias must be applied to this terminal

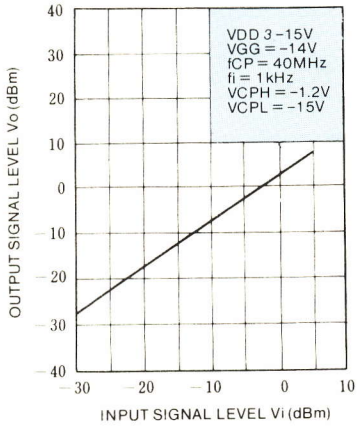
Circuit Diagram



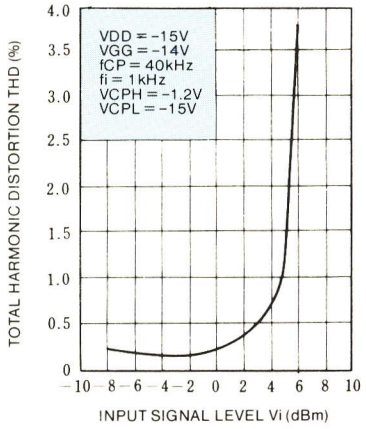
Vo – VI



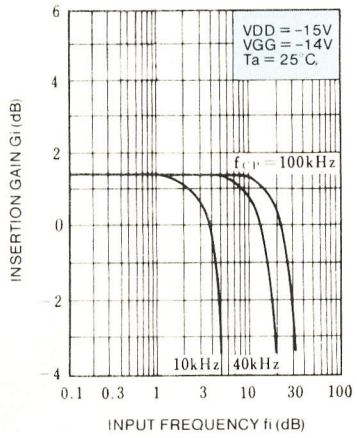
Vo – Vi



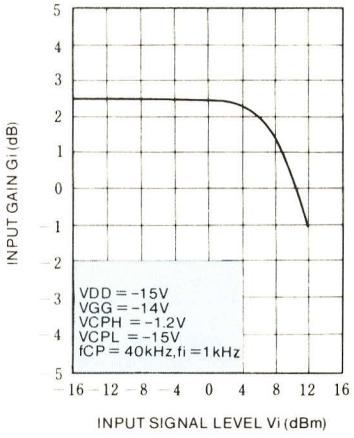
THD – Vi



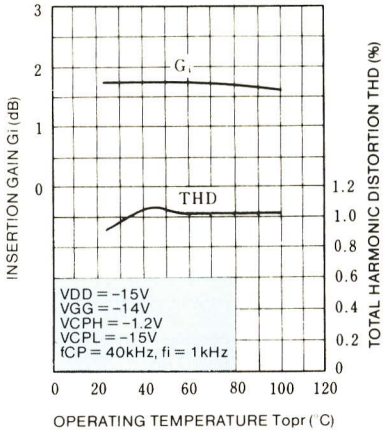
Gi – fi



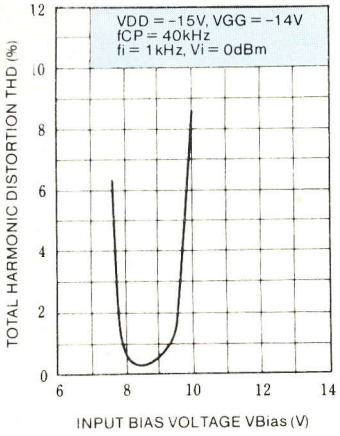
Gi – Vi



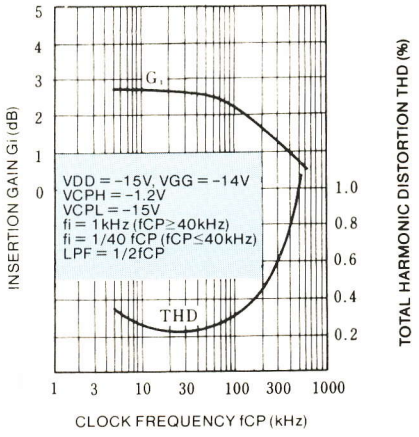
Gi, THD – Topr



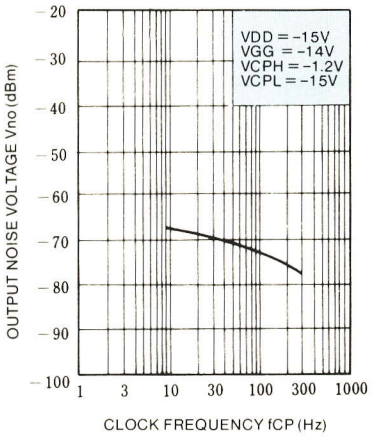
THD – VBias



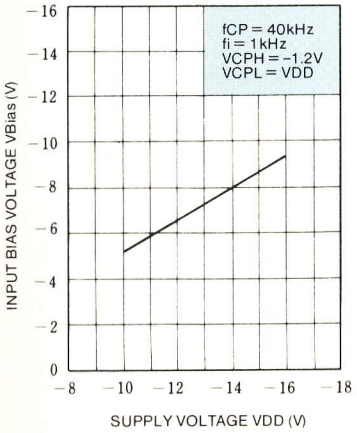
Gi, THD – fCP



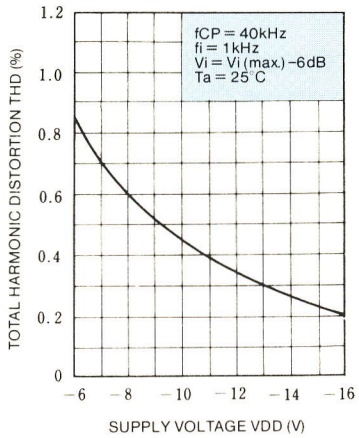
Vno – fCP



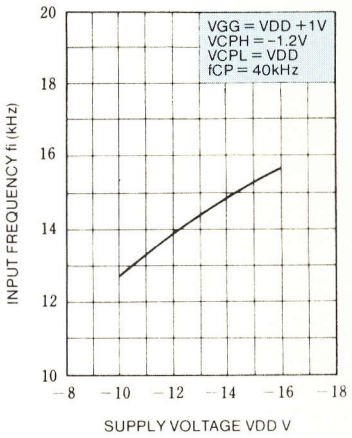
VBias – VDD



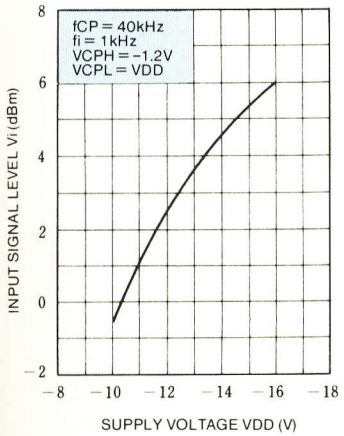
THD – VDD



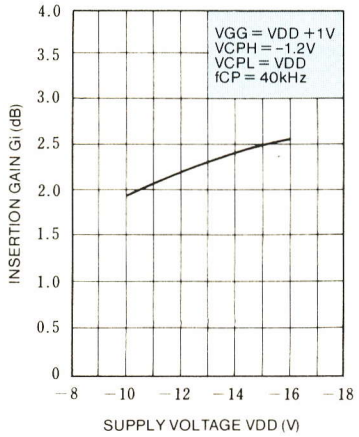
fi – VDD



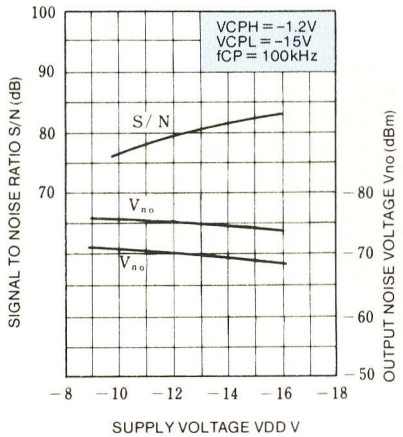
Vi – VDD



Gi – VDD



S/N, Vno – VDD



MN3012

BBD With 3 Parallel Signal Delay Lines Incorporating Clock Generator

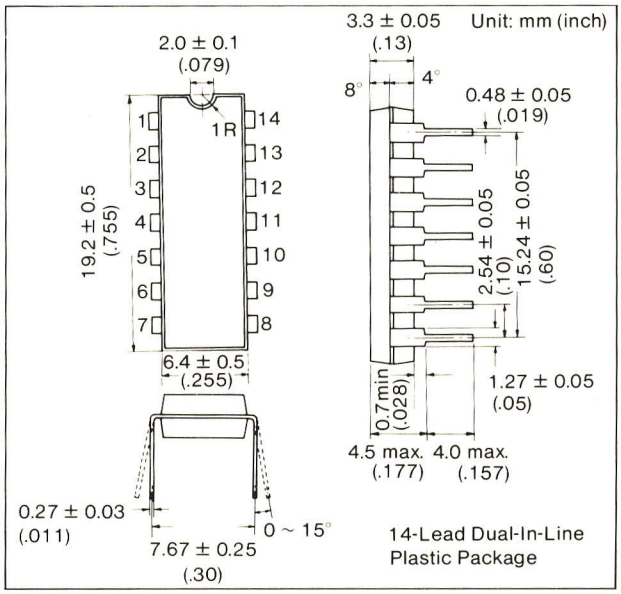
General Description

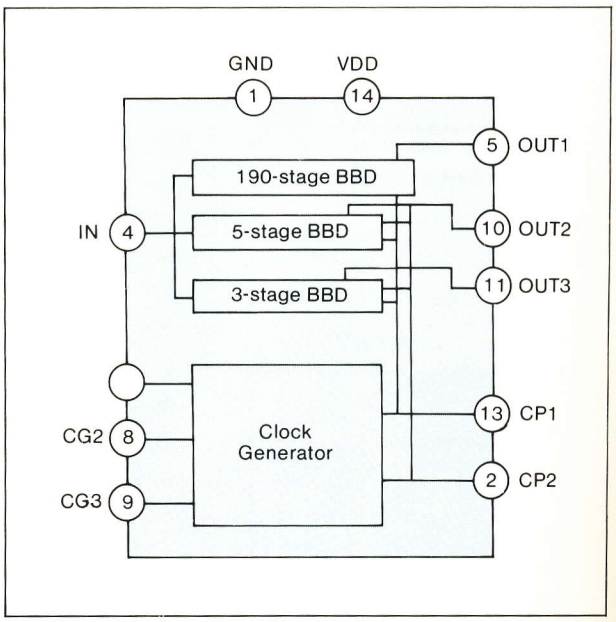
The MN3012 is BBD provided with 3, 5, 190 stages three parallel delay lines and a clock generator. The clock frequency which determines a delay time is controlled by the value of external resistor and capacitor connected to CG1, CG2 and CG3 terminals.

The MN3012 provides three differently delayed signals on OUT1, OUT2 and OUT3 terminals. The device is particularly suitable for producing chorus, vibrato and reverberation effects of audio equipment.

Features:

1. −8.5 −15V single voltage supply (VDD)
2. Delay time 01 : 0.475 − 9.5ms (190-stage)
   02 : 0.0125–0.25 (5-stage)
   03 : 0.0075–0.15 (3-stage)
3. Dynamic range S/N = 98dB typ. (OUT3)
4. Insertion IL = 0 dB typ.
5. Distortion THD = 0.4% typ.
6. Incorporating clock generator
7. Clock frequency 10–200KHz
8. Clock component cancellation
9. P-channel silicon gate process.





Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	VDD, VI, VO, Vcp	−18~+0.3	V
Operating Temperature	Topr	−20~+70	°C
Storage Temperature	Tstg	−56~+125	°C

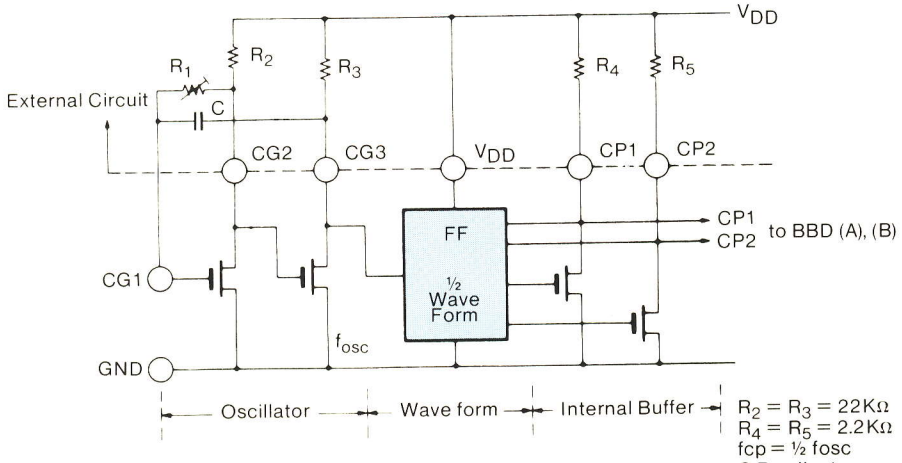
Operating Conditions (Ta = 25C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	VDD	−6.5	−15	−16	V
Clock H Level	VcpH	0		−0.4	V
Clock L Level	VcpL		VDD		V
Clock Frequency	fcp	10		200	KHz
Clock Input Capacitance	Ccp			180	pF
Input DC Bias	Vbias				V

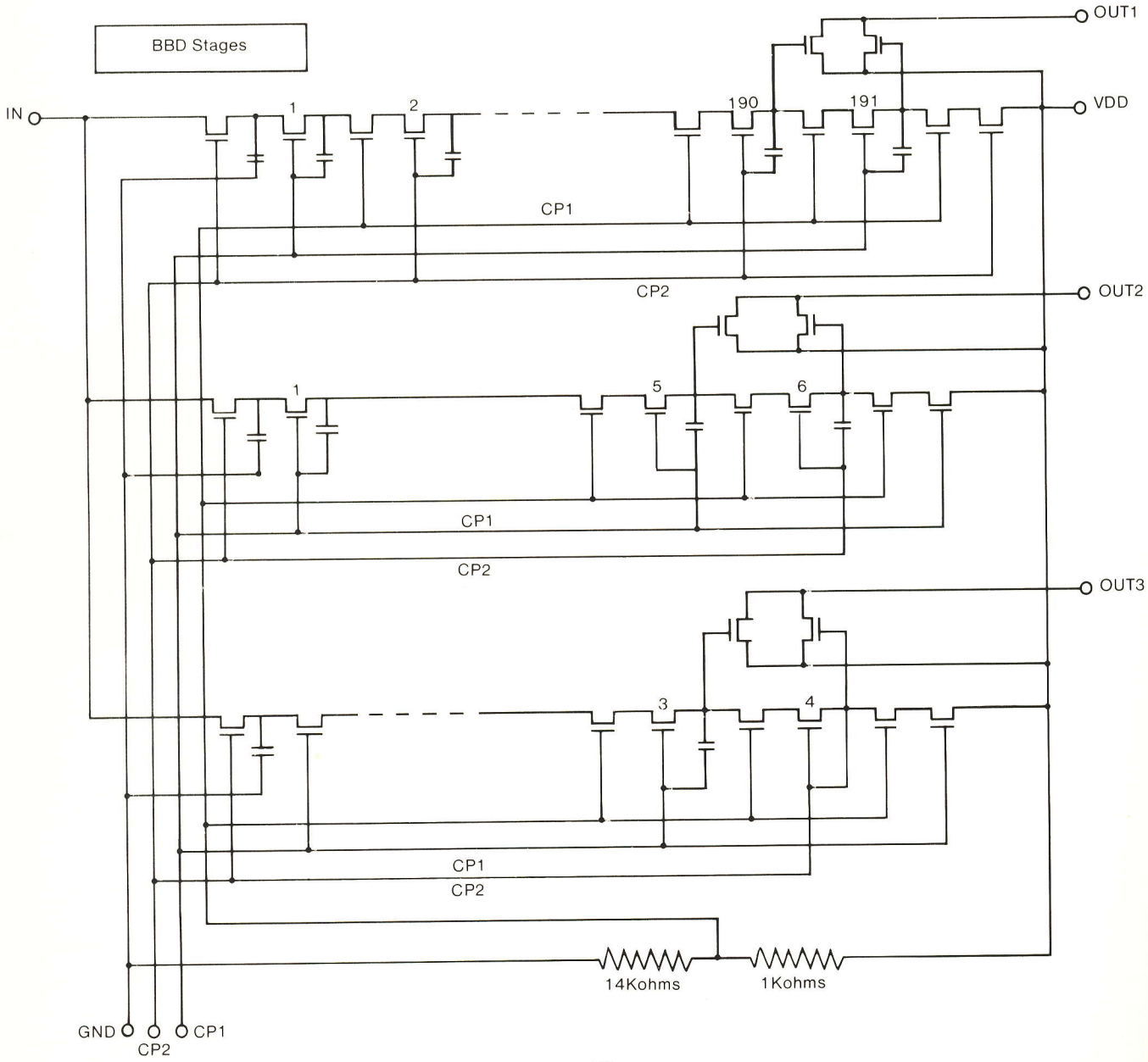
Characteristics (Ta = 25°C, VDD = −15V, VcpL = −15V, VcpH = OV, RL = 56Kohms, C = 100pF R1 = R3 = 22 Mohms, R4 = R5 = 2.2Kohms, fcp = 1/2 fosc (R1 adjust)

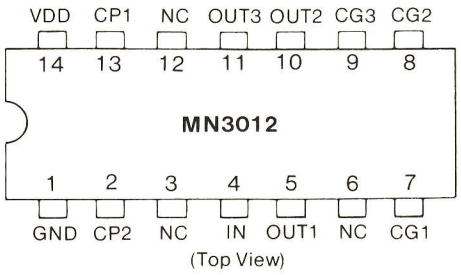
Item	Symbol	Condition	Min.	Typ.	Max.	°Unit
Signal Delay Time OUT1 Terminal OUT2 Terminal OUT3 Terminal	 tD1 tD2 tD3	 fcp = 10KHz 200KHz	 0.475 0.0125 0.0075		 9.5 0.125 0.15	 ms ms ms
Input Signal Frequency OUT Terminal 1 OUT Terminal 2 OUT Terminal 3	 fin1 fin2 fin3	 fcp = 40KHz Output −3dB			 12 14 15	 KHz KHz KHz
Input Signal Voltage	vin	THD = 2.5%			1.2	Vrms
Insertion Loss	IL	fcp = 40KHz fin = 1KHz vin = 0.775 Vrms		0		dB
Distortion	THD			0.4		%
Noise Voltage OUT Terminal 1 OUT Terminal 2 OUT Terminal 3	 Vn1 Vn2 Vn3	 fcp = 100KHz Weighted by A curve			 0.14 0.05 0.04	 mVrms mVrms mVrms
S/M Ratio OUT Terminal 1 OUT Terminal 2 OUT Terminal 3	 S/N1 S/N2 S/N3	 Vn/Vin fcp = 100KHz Weighted by A curve		 90 97 98		 dB dB dB

Circuit Diagram
Clock Generator



Note: When external clock is used, remove R1 and C, apply the clock input to CG1.



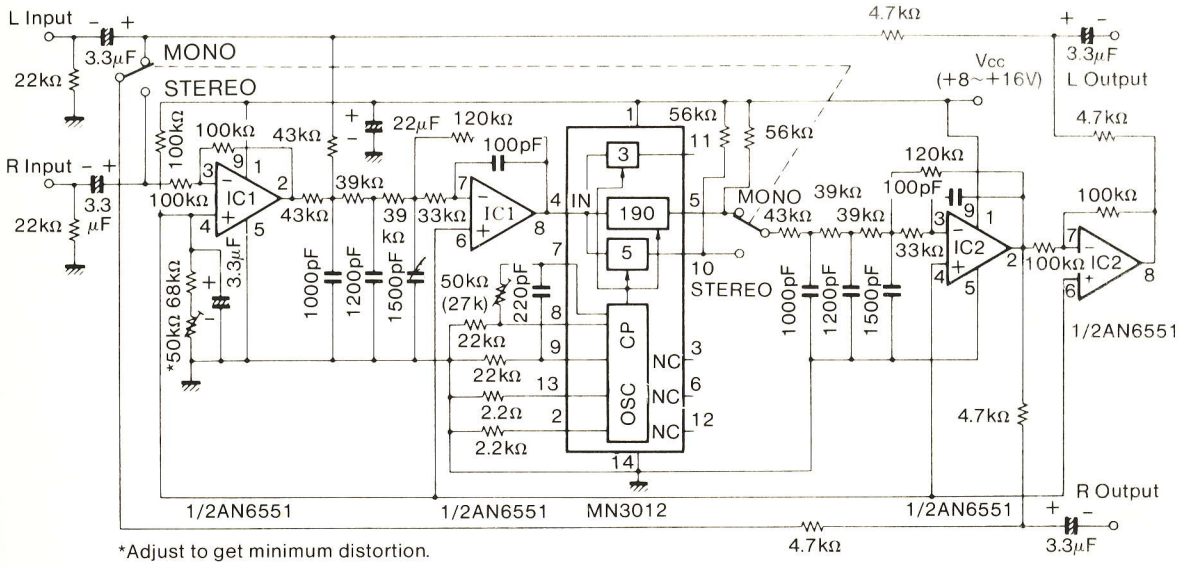


(Top View)

Terminal Assignments

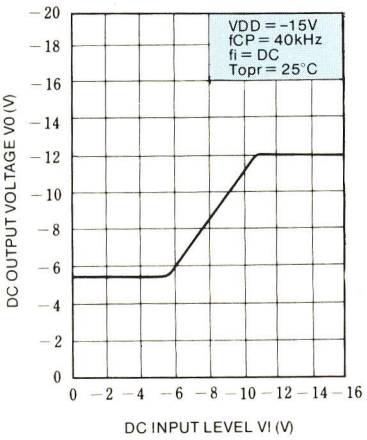
Pin No.	Symbol	Terminal
1	GND	Grounding
2	CP2	Clock pulse input
4	IN	Analog signal input
5	OUT1	Output terminal at 190 and 191-stage
7	CG1	Clock oscillation input
8	CG2	Clock oscillation input
9	CG3	Clock oscillation input
10	OUT2	Output terminal at 5 and 6-stage
11	OUT3	Output terminal at 3 and 4-stage
13	CP1	Clock pulse input
14	VDD	VDD = -15V supply terminal

Note: Terminal No. 3, 6, and 12 are non connection

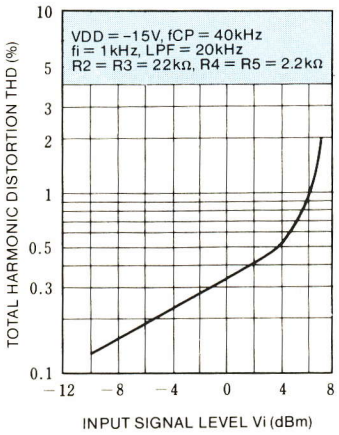


*Adjust to get minimum distortion.

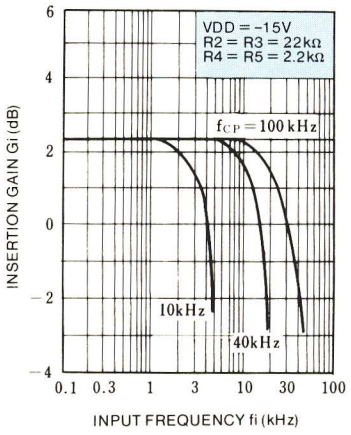
$V_O - V_I$



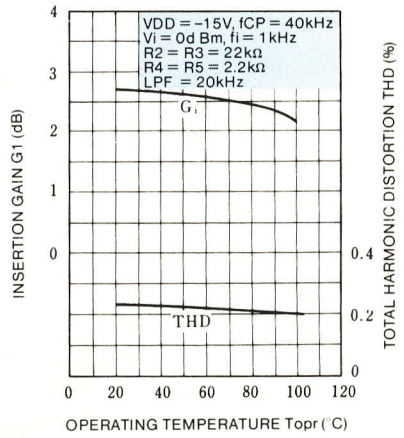
THD – V_i



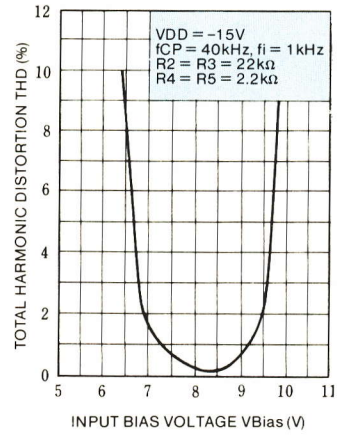
$G_i - f_i$



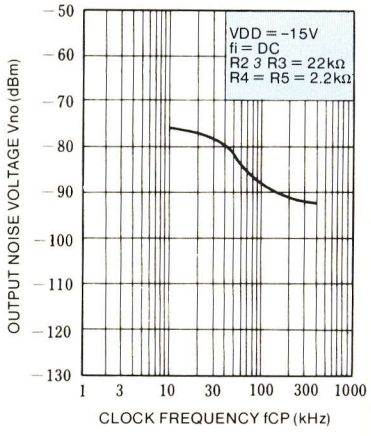
G_i, THD – T_{opr}



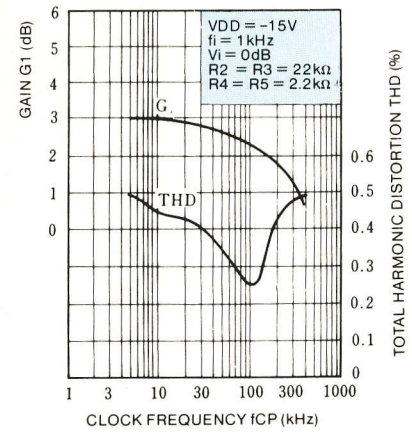
THD – V_{Bias}



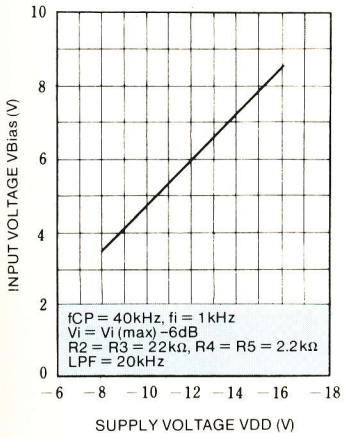
$V_{no} - f_{CP}$



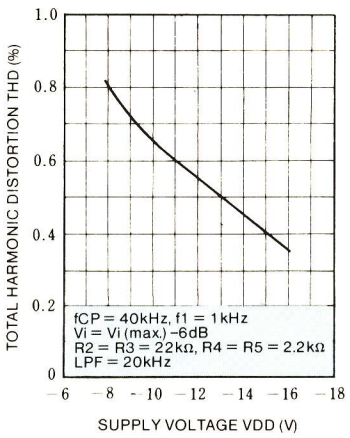
G_i, THD – f_{CP}



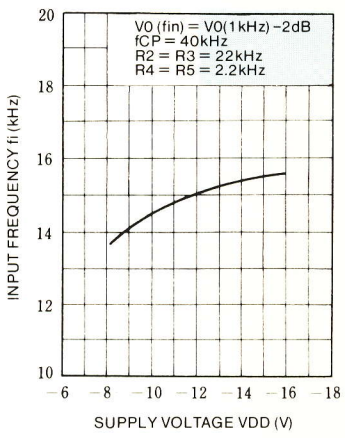
$V_{Bias} - V_{DD}$



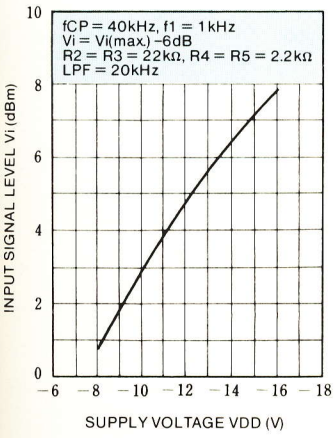
THD – V_{DD}



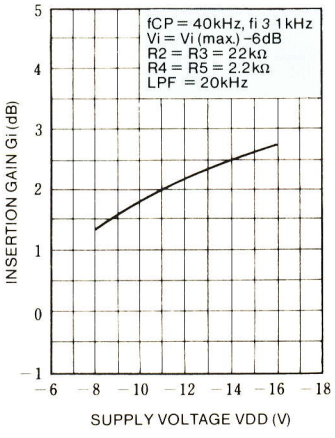
$f_i - V_{DD}$



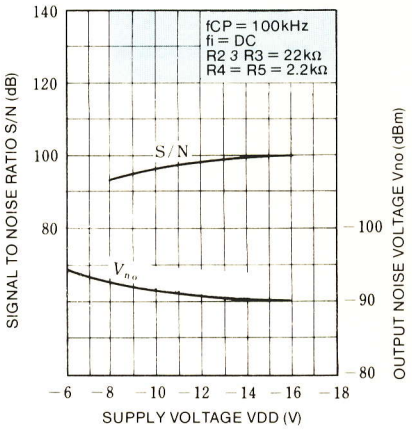
$V_i - V_{DD}$



$G_i - V_{DD}$



S/N, $V_{no} - V_{DD}$



MN3101

Clock Generator / Driver MN 3101 for BBD's

General Description

The MN3101 is a CMOS integrated circuit designed to generate low impedance two clock phases required for driving BBD's. In addition, the MN3101 provides the optimum VGG for BBD's* when the MN3101 is used with BBD's on a common VDD supply.

The self-contained oscillator can be controlled by an external RC circuit, but an external oscillator can also be used. The clock frequency is 1/2 of the oscillation frequency.

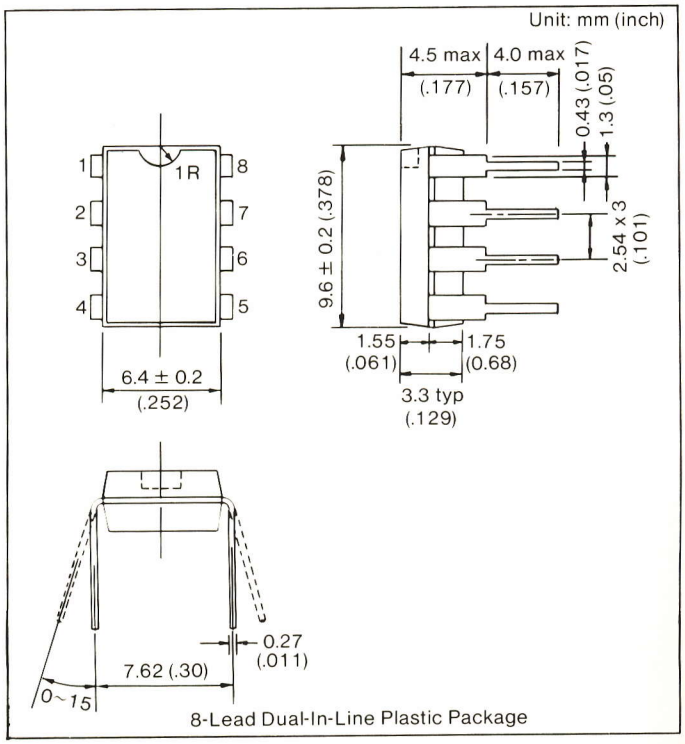
*PANASONIC's BBD product range: MN3001, MN3002, MN3003, MN3004, MN3005, MN3006, MN3007, MN3008, MN3009, MN3010, MN3011, MN3012. Note: The MN3003 is provided with an internal oscillator.

Features:

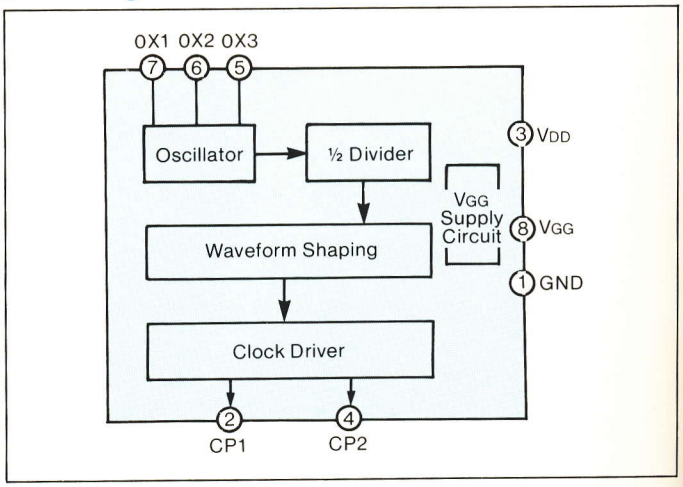
- **BBD direct driving capability – up to two MN3005 types (equivalent to 8192 stages).**
- **Either internal or external oscillator can be used**
- **Two phases (1/2 duty) output**
- **Provided with VGG supply circuit**
- **Operates on a single power supply: – 8 ~ –16V**
- **8-lead dual-in-line plastic package**

Application

- **BBD clock generator/driver**



Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Supply Voltage	V_{DD}	−18~+0.3 *	V
Input Terminal Voltage	V_I	V_{DD} − 0.3~+0.3 *	V
Output Terminal Voltage	V_O	V_{DD} − 0.3~+0.3 *	V
Power Dissipation	P_D	200	mW
Operating Temperature	Topr	−10~+70	°C
Storage Temperature	Tstg	−30~+125	°C

*With respect to GND = OV.

Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	GND = OV	−8	−15	−16	V

Electrical Characteristics (Ta = 25°C, V_{DD} = −15V, GND = OV)

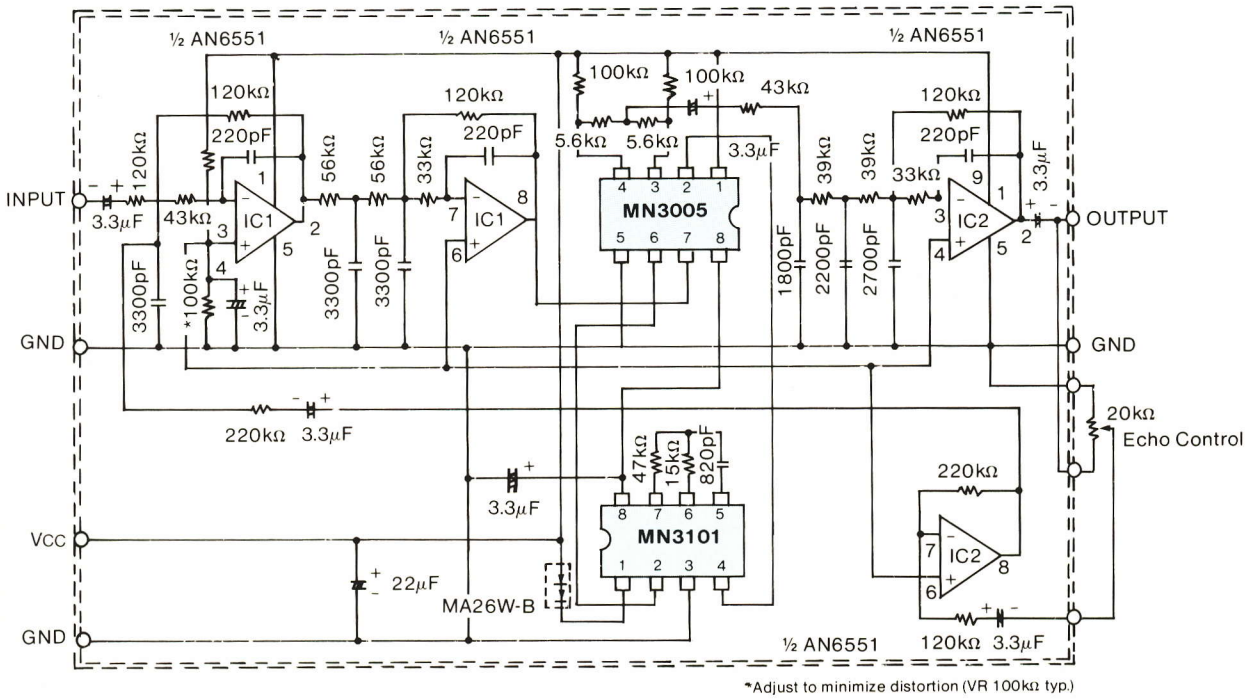
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	I_{DD}	Without load		3		mA
Power Consumption	Ptot	Clock output 40kHz		45		mW
OX1 Input Terminal						
Input Voltage "H" Level	V_{IH}		0		−1	V
Input Voltage "L" Level	V_{IL}		V_{DD}+1		V_{DD}	V
Input Leakage Current	I_{LK}	V_I = 0~−15V			30	μA
OX2 Output Terminal						
Output Current "H" Level	I_{OH1}	V_O = −1.0V	0.6			mA
Output Current "L" Level	I_{OL1}	V_O = −14V	0.5			mA
Output Leakage Current	I_{LOL1}	V_O = V_{DD}			30	μA
Output Leakage Current	I_{LOH1}	V_O = GND			30	μA
OX3 Output Terminal						
Output Current "H" Level	I_{OH2}	V_O = −1.0V	1.5			mA
Output Current "L" Level	I_{OL2}	V_O = −14V	2.0			mA
Output Leakage Current	I_{LOL2}	V_O = V_{DD}			30	μA
Output Leakage Current	I_{LOH2}	V_O = GND			30	μA
CP1, CP2 Output Terminal						
Output Current "H" Level	I_{OH3}	V_O = −1.0V	10			mA
Output Current "L" Level	I_{OL3}	V_O = −14V	10			mA
Output Leakage Current	I_{LOL3}	V_O = V_{DD}			30	μA
Output Leakage Current	I_{LOH3}	V_O = GND			30	μA
V_{GG} Output Terminal*						
Output Voltage	$V_{GG\ OUT}$			−14.0		V

*This terminal outputs VGG voltage particularly suitable for the BBD's manufactured by PANASONIC. The voltage is not necessarily suitable for the manufacturer's products.

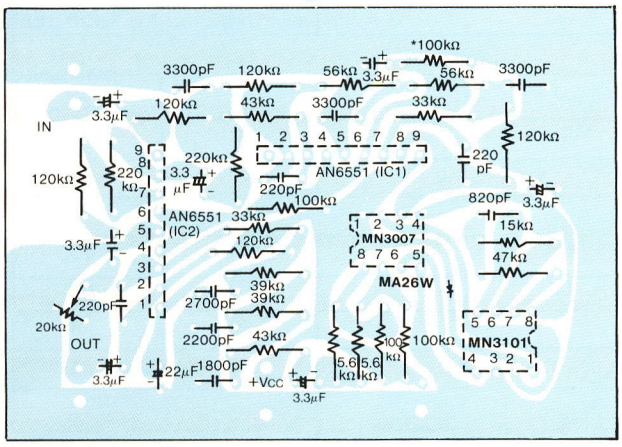
The $V_{GG\ OUT}$ changes depending on V_{DD}. The relationship between $V_{GG\ OUT}$ and V_{DD} is as follows:

VGG OUT = 14/15 VDD

Application Circuit Example 1 – Echo Effect Generation Circuit With The MN3005



Printed Circuit Board Layout (Actual Size)



Quick Reference Data for The MN3005

Item	Symbol	Value	Unit
Supply Voltage	VDD. VGG	−15. VDD +1	V
Signal Delay Time	tD	20.48 ~ 204.8	msec.
Total Harmonic Distortion	THD	1	%
Signal to Noise Ratio	S/N	75	dB

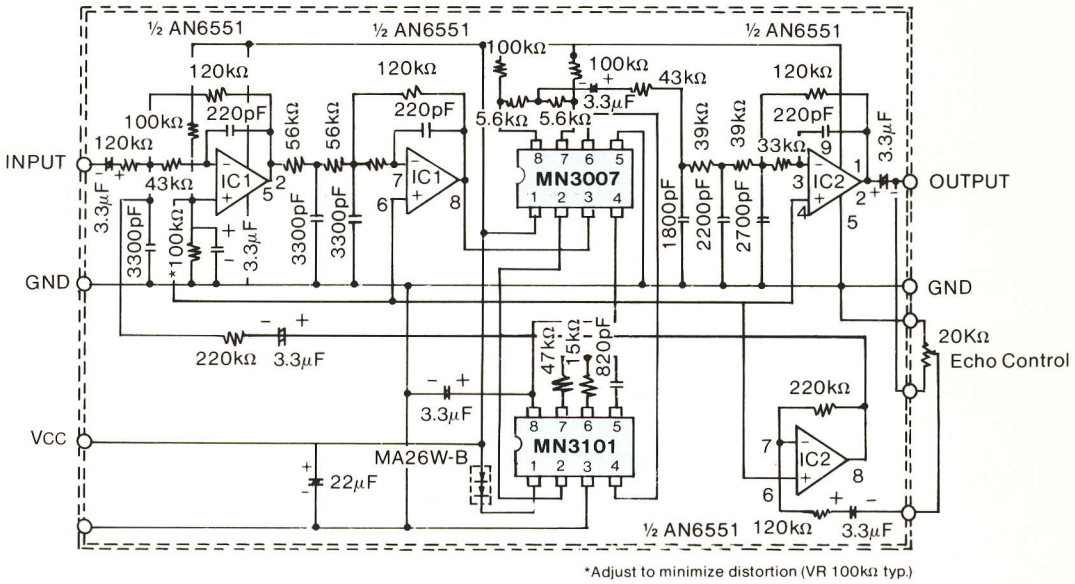
Quick Reference Data for the AN6551

Item	Symbol	Value	Unit
Supply Voltage	VCC	15	V
	VEE	−15	V
Input Bias Current	IB	500max.	nA
Voltage Gain	Gv	100typ.	dB
Noise Voltage Referred to Input	Vni	2.5typ.	μVrms
Maximum Output Voltage	Vo(max.)	±13typ.	V
Common-Mode Rejection Ratio	CMR	90typ.	dB
Supply Voltage Rejection	SVR	30typ.	μV/V

Electrical Characteristics of The Application Circuit Using The MN3005 (Vcc = 9V, Ta = 25°C)

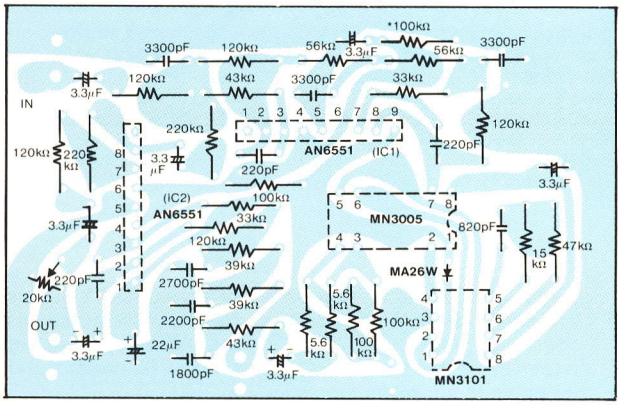
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	ICC			8	10	mA
Total Power Consumption	Ptot			70		mW
Signal Delay Time	tD	fcp = 18±2kHz	100	113	128	msec
Cutoff Frequency	fco			2		kHz
Input Signal Swing	Vi	THD = 2.5%			500	mVrms
Insertion Loss	Li	fi = 1kHz, Vi = 300mV	−2	0	2	dB
Total Harmonic Distortion	THD	Fi = 1kHz, Vi = Vi(max.) −6dB		0.5	1	%
Output Noise Voltage	Vno	Vi = OV			0.35	mVrms
Signal to Noise Ratio	S/N	Vs Vi(max.) = 500mVrms	60			dB

Application Circuit Example 2 – Echo Effect Generation Circuit With The MN3007



*Adjust to minimize distortion (VR 100kΩ typ.)

Printed Circuit Board Layout (Actual Size)



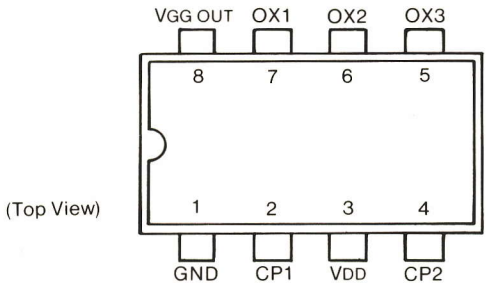
Quick Reference Data for The MN3007

Item	Symbol	Value	Unit
Supply Voltage	VDD. VGG	−15, V_{DD} +1	V
Signal Delay Time	tD	5.12 ~ 51.2	msec.
Total Harmonic Distortion	THD	0.3	%
Signal to Noise Ratio	S/N	88	dB

Electrical Characteristics of The Application Circuit Using The MN3007 (Vcc = 9V, Ta = 25°C)

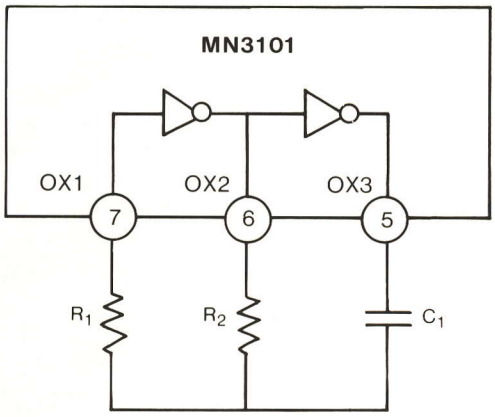
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current	ICC			8	10	mA
Total Power Consumption	Ptot			70		mW
Signal Delay Time	tD	fcp = 14±2kHz	32	37	43	msec
Cutoff Frequency	fco			2		kHz
Input Signal Swing	Vi	THD = 2.5%			500	mVrms
Insertion Loss	Li	fi = 1kHz, Vi = 300mV	−2	0	2	dB
Total Harmonic Distortion	THD	fi = 1kHz, Vi = Vi(max.) −6dB		0.5	1	%
Output Noise Voltage	Vno	Vi = OV			0.35	mVrms
Signal to Noise Ratio	S/N	Vs Vi(max.) = 500mVrms	60			dB

Terminal Assignments



Pin No.	Symbol	I/O	Functions	
1	GND	Supply	Grounding	
2	CP1	O	Outputs 1/2 duty cycle clock pulse at frequency 1/2 of an oscillation frequency, having an opposite phase relationship with respect to CP2.	
3	V_{DD}	Supply	−15V supply voltage input.	
4	CP2	O	Outputs clock pulse having an opposite phase relationship with respect to CP1.	
5	OX3	O	Internal Oscillation:	External Oscillation:
6	OX2	O	C R network connection to the pins	An external oscillation input to OX1.
7	OX1	I	(See oscillator circuit example)	with OX2 and OX3 open.
8	$V_{GG\ OUT}$	O	−14V output (When V_{DD} = 15V) The relationship between V_{DD} and $V_{GG\ OUT}$ is: V_{GG} OUT = 14/15 V_{DD}	

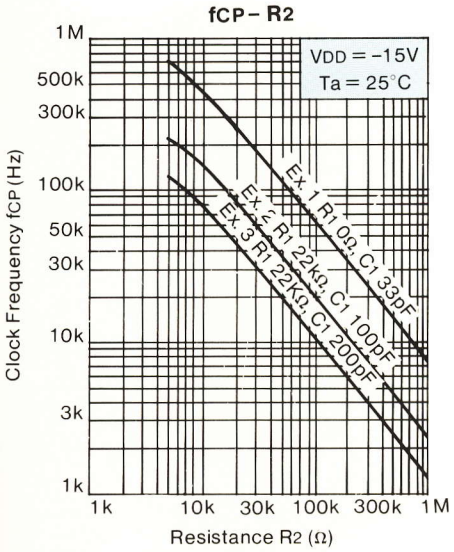
Oscillator Circuit Example

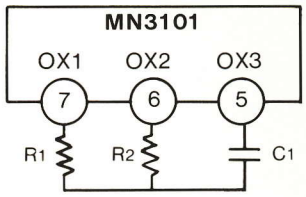


The internal oscillation circuit of the MN3101 consists of a 2-stage inverter. The oscillation frequency is established by the time constant of C_1 and R_2. The following table shows examples of C_1, R_1 and R_2 values. Fcp − R_2 characteristics example is shown in Figure 1.

Example \ Constant	R1 (Ω)	R2 (Ω)	C1 (pF)	f osc** (kHz)	F CP* (kHz)
Example 1	0	5k~1M	33	15~1500	7.5~750
Example 2	22k	5k~1M	100	5.2~440	2.6~220
Example 3	22k	5k~1M	200	1.4~280	0.7~140

*Clock output frequency for CP1 or CP2.
**Oscillation frequency for OX1, OX2, and OX3.





Maximum Clock Frequency

The maximum clock frequency is limited by device power dissipation and load capacitance. The power consumption of the devices increases as the clock frequency or load capacitance is increased (See Fig. 2). Therefore, a proper clock frequency and load capacitance value must be chosen so that the maximum allowable power dissipation of 200mW for the MN3101 is not exceeded.

Fig. 3 shows the relationship between the maximum frequency and load capacitance for 150mW power dissipation. The maximum clock frequency can be increased without increasing the power consumption when a resistor is connected to each clock output terminal (See Fig. 2 and 3). The series resistor consumes a part of the power required for driving the load capacitance and help reduce the power dissipated in the device.

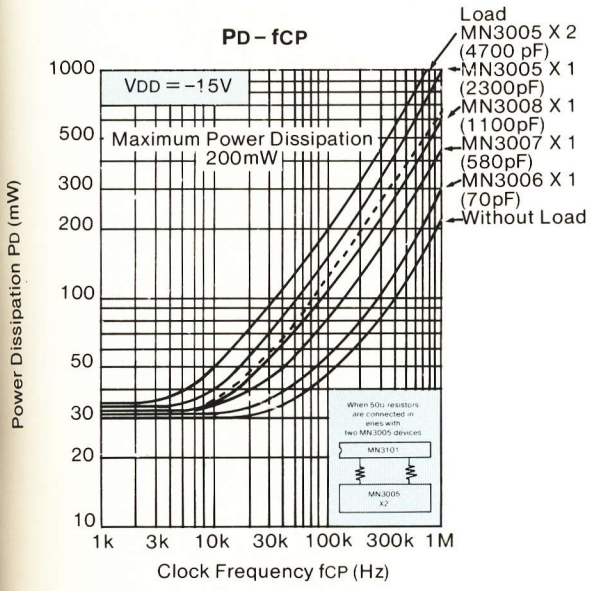


Fig. 2 Power Consumption vs Clock Frequency

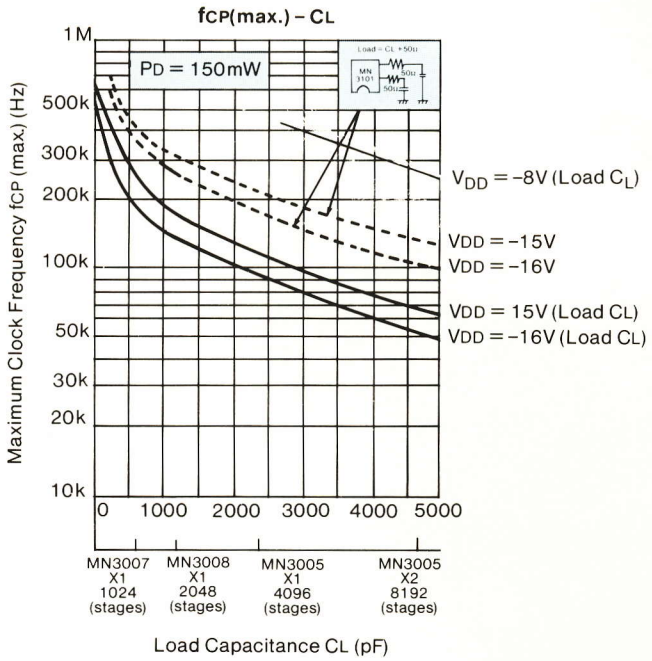
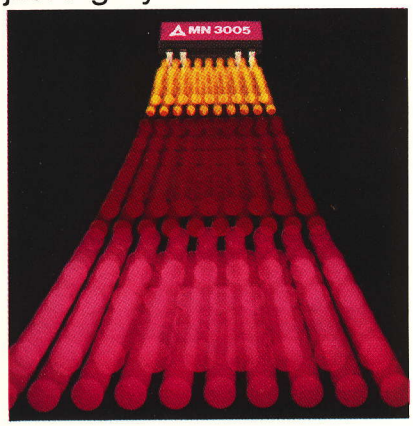


Fig. 3 Maximum Clock Frequency vs Load Capacitance at 150mW Power Consumption

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