Designer's Guide to:
Op-amp booster stages—Part 1

# Boost op-amp output without sacrificing drift and gain specs

*Many applications require greater output power than most monolithic op amps can deliver. When you need augmented voltage or current gain (or both) from low-power amplifiers, you must add separate output stages, such as the ones described in this, the first article of a 2-part series. However, an output stage's added gain and phase shift can cause poor ac response or outright oscillation unless you judiciously apply the frequency-compensation methods that part 2 will discuss.*

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Standard IC processing techniques limit the total power-supply span for most monolithic op amps to 36 volts, thus limiting available output swing. In addition, supplying current beyond tens of milliamperes requires large output transistors, which dissipate more power than most IC op amps can handle. To attain greater outputs from these limited-voltage and -current amplifiers, you must add a power-gain stage.

This booster stage usually sits within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics. But when an output stage resides in the amplifier's feedback path, you must be concerned with the feedback loop's stability; part 2 of this series (scheduled for June 12) will discuss frequency-compensation considerations.

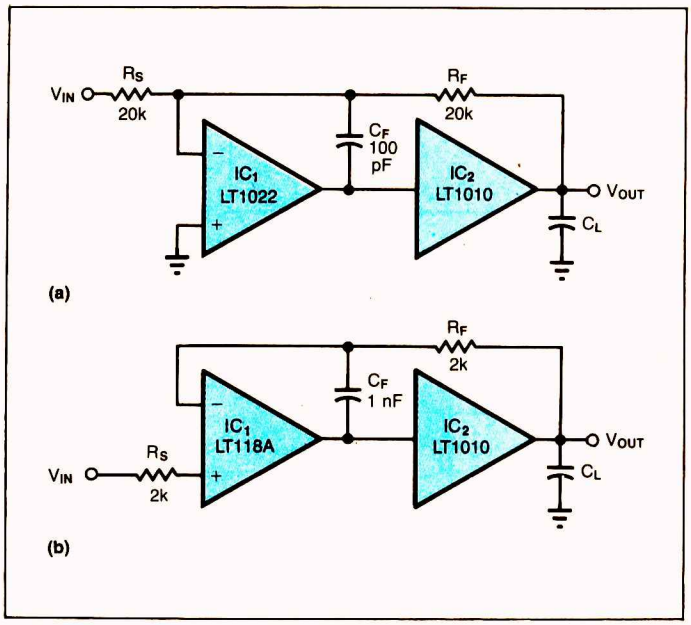



***Fig 1—The interstage capacitor, $C_F$,** shorts out the feedback loop at high frequencies so that phase shift from the load's capacitance won't cause loop instability.*

The circuitry needed in an output stage varies with the application. Current and voltage boosting are common requirements, and both are often simultaneously required. Voltage-gain stages usually mandate high-voltage power supplies, but output stages that generate their own high voltages are an alternative.

**Fig 1a** shows the LT1010 monolithic 150-mA current

*Usually, the booster stage is within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.*

booster residing within the feedback loop of a fast FET amplifier. At low frequencies, the buffer's offset-voltage and gain errors are negligible. At higher frequencies, $C_F$ shorts out the feedback loop so that phase shift from the load capacitance acting with the buffer's output resistance doesn't cause loop instability. At high frequencies, the buffer amp is, in effect, out of the op amp's feedback loop. The LT1010 is particularly adept at driving large capacitive loads such as cables.

$C_F$ reduces small-signal bandwidth, but you can obtain considerable load isolation without reducing bandwidth below the power bandwidth. (It's common to require a bandwidth reduction to filter high-frequency noise or unwanted signals, in any case.) The follower configuration **(Fig 1b)** is unique in that the circuit achieves capacitive-load isolation without a reduction in small-signal bandwidth, though the output impedance of the buffer comes into play at high frequencies. This precision unity-gain buffer has a 10-MHz bandwidth without capacitive loading, yet it's stable for load capacitance as high as 0.3 μF.

Both circuits in **Fig 1** will deliver 150 mA of output current. The LT1010 supplies short-circuit and thermal-overload protection. The op amp you select sets the slew limit.

**Fig 2** uses a discrete stage to provide a 3A-output capability. The configuration shown provides a clean, quick way to increase the LT1010's output power. The circuit proves useful for high-current loads, such as linear-actuator coils in disk drives.

The grounded 100Ω resistor supplies a load for the LT1010 while the 33Ω resistors sense the LT1010's supply current. The voltage drop across the 33Ω resistors biases $Q_1$ and $Q_2$. The other 100Ω resistor closes a local feedback loop, stabilizing the output stage. Feedback to the LT1056 control amplifier is via the 10-kΩ resistor. $Q_3$ and $Q_4$, sensing across the 0.18Ω resistors, furnish current limiting.

The output transistors have low $f_T$ and need no special frequency compensation. The 68-pF capacitor

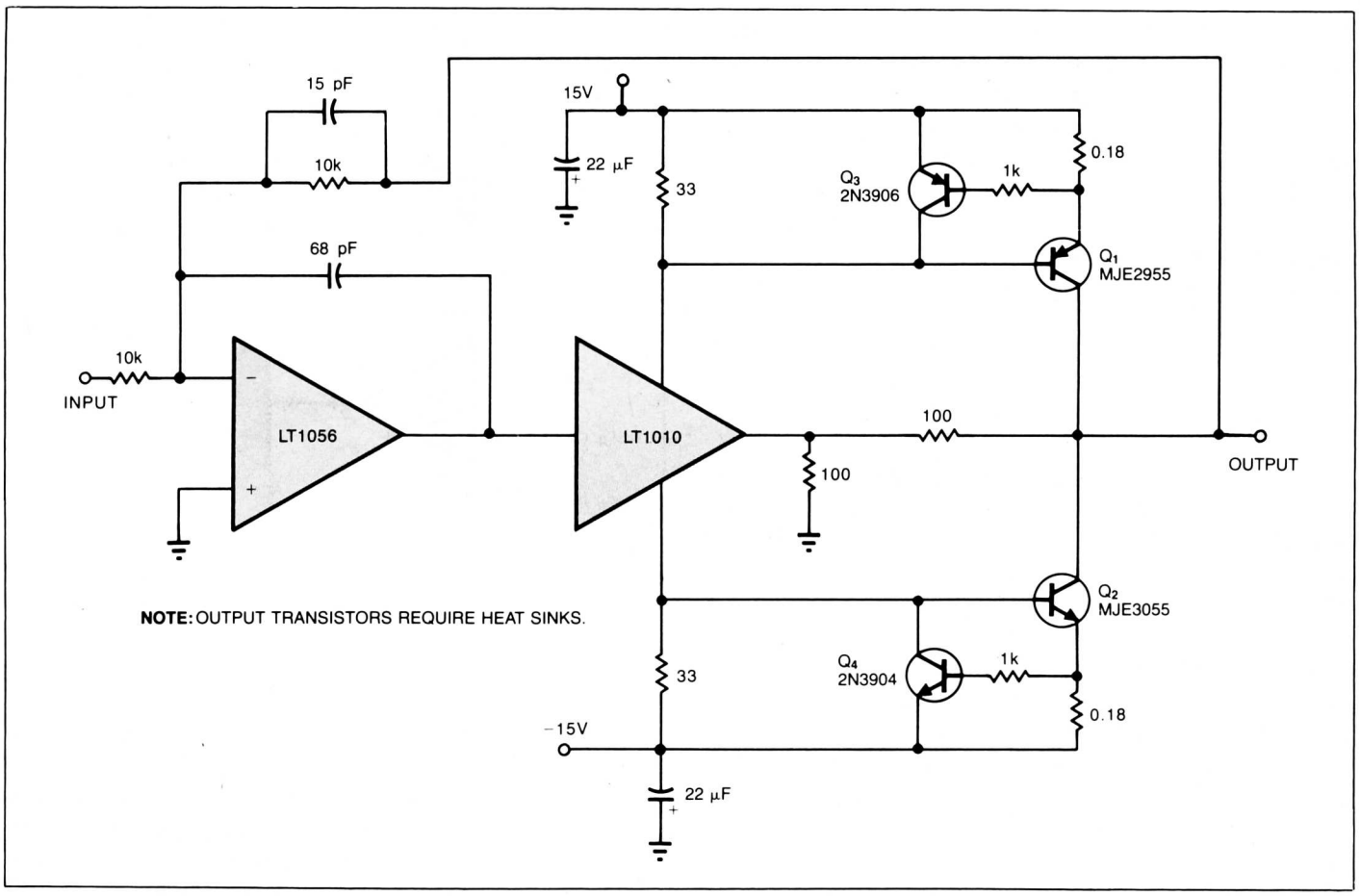



***Fig 2—This circuit provides a clean, quick** way to increase the op amp's output power to 3A.*

rolls off the frequency response of the LT1056 for dynamic stability, and the 15-pF feedback capacitor trims edge response. At full power (±10V, 3A pk), bandwidth is 100 kHz and slew rate is about 10V/μsec. Harmonic distortion measures below 1% at 1 kHz.

The circuit in **Fig 3** features higher power and has lower harmonic distortion—about 0.05%. This discrete stage provides a 5A-output capacity. Current sources $Q_1$ and $Q_2$ bias the complementary Darlington output transistors, $Q_3$ and $Q_4$. The dashed lines indicate that $Q_3$ and $Q_4$ must be in physical contact with the 1N914 diodes for thermal mating, allows the transistors' biasing to track over temperature, avoiding thermal runaway in the output stage. Note also that $Q_3$ and $Q_4$ require heat sinks. $Q_5$ and $Q_6$ limit current by diverting drive from the output-stage transistors' bases. The transistors' $V_{BE}$ turn-on voltage (about 0.6V) across the 0.1Ω shunts sets a 6A current limit.

### Diodes provide temperature compensation

The Darlington transistors have low $f_T$, and the stage exhibits low frequency response. The 39-pF capacitor rolls off the LT1055's frequency response locally for dynamic stability. This compensation permits overall response approaching that of the op amp alone. At full power (±10V, 5A pk), bandwidth is 100 kHz and slew rate is about 10V/μsec.

All the circuits discussed so far place the output

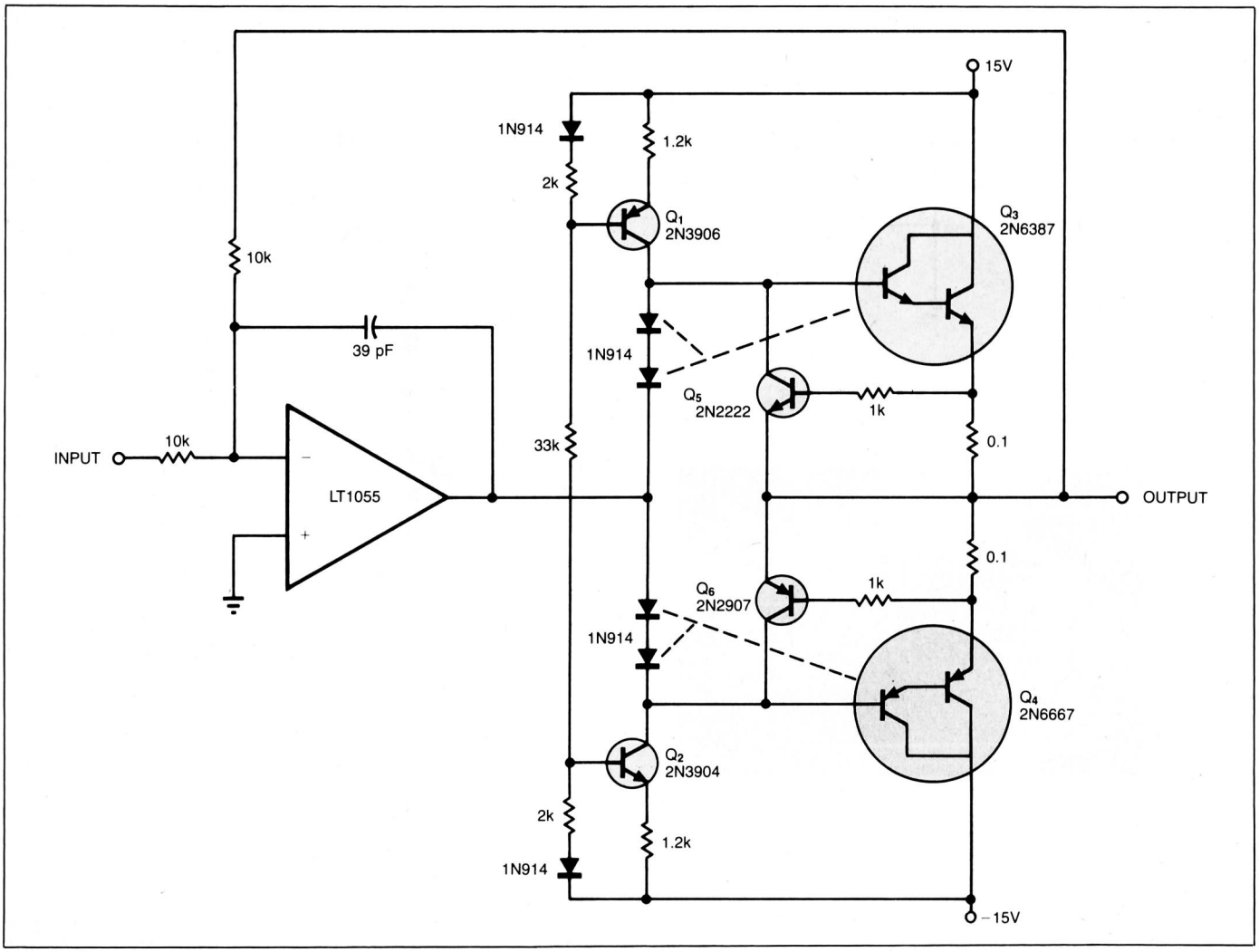



***Fig 3—Providing a 5A output, this circuit*** *also features harmonic distortion of 0.05%. The dashed lines indicate that the diodes and transistors must be thermally mated to prevent thermal runaway.*

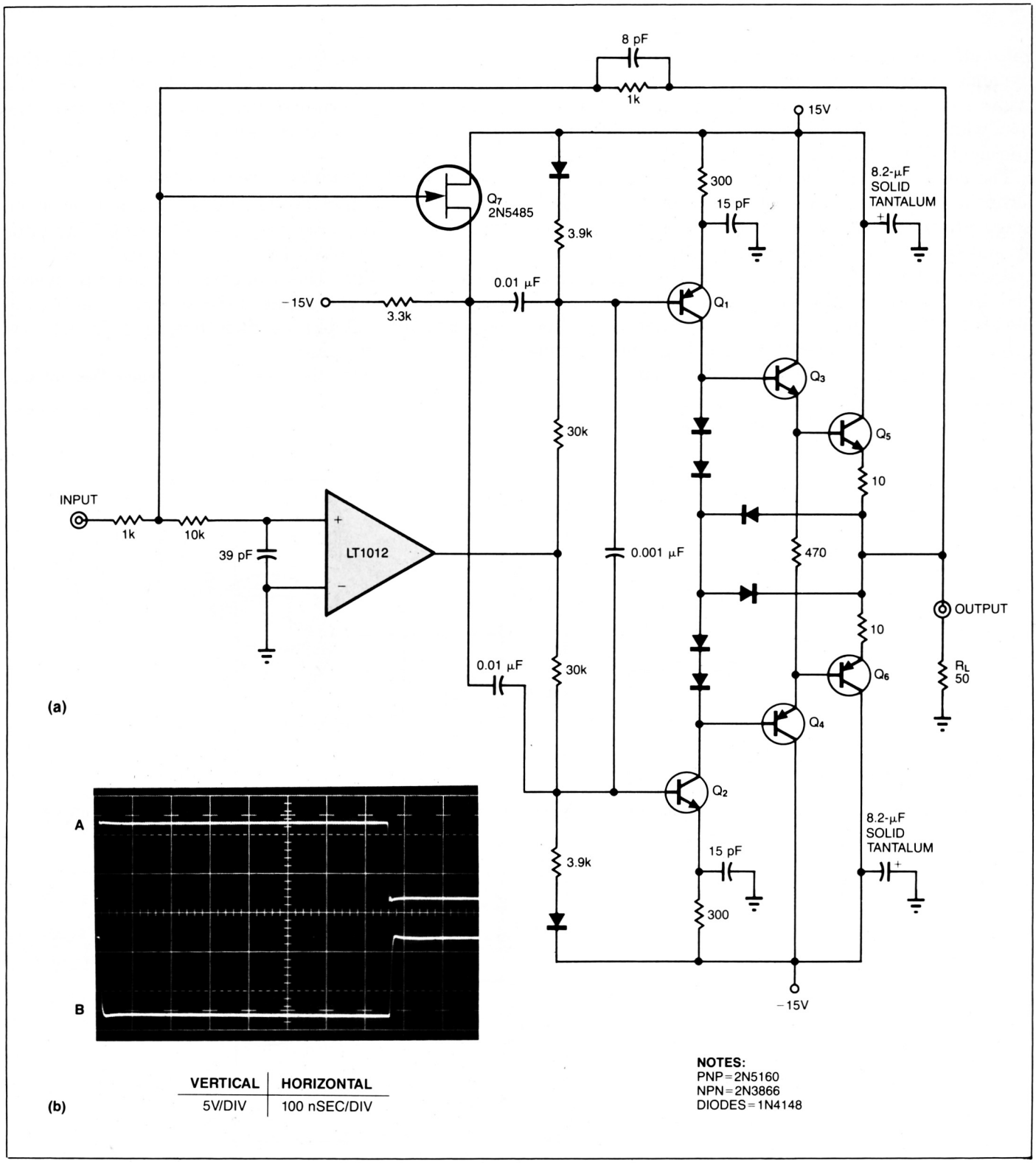



***Fig 4—Using a feed-forward technique,*** *this wideband booster stage* ***(a)*** *exhibits low drift and gain stability. The circuit features a slew rate in excess of 1000V/μsec and a full-power bandwidth of 7.5 MHz. The scope photo* ***(b)*** *shows the circuit driving a 10V pulse into a 50Ω load. Trace A is the input and trace B is the output.*

*Voltage-gain stages usually mandate high-voltage power supplies, but output stages that generate their own high voltages are an alternative.*

stage's booster within the op amp's feedback loop. Although this placement ensures low drift and good gain stability, the op amp's response limits speed. **Fig 4a** shows a very wideband, current-boost stage. The LT1012 corrects dc errors in the booster stage, but doesn't amplify high-frequency signals. $Q_7$ and the 0.01-μF coupling capacitors feed fast signals directly to the output stage.

DC and low-frequency signals, on the other hand, drive the stage via the op amp's output. This parallel-path approach allows very broadband performance without sacrificing the dc stability of the op amp, thus boosting the LT1012's output current and speed.

The output stage consists of current sources $Q_1$ and $Q_2$ driving the $Q_3/Q_5$ and $Q_4/Q_6$ complementary emitter followers. The transistors specified have $f_T$ approaching 1 GHz, resulting in a very fast stage. The diode network at the output steers drive current away from the transistor bases when output current exceeds 250 mA, providing fast short-circuit protection.

Net inversion in the stage means the feedback must return to the LT1012's positive input. The circuit's high-frequency summing node is the junction of the 1-kΩ and 10-kΩ resistors at the LT1012. The 10-kΩ/39-pF pair filters high frequencies, permitting accurate dc summation at the LT1012's positive input. The low-frequency rolloff of the fast stage matches the high-frequency characteristics of the LT1012 section, minimizing aberration in the circuit's ac response. The 8-pF feedback capacitor optimizes settling characteristics at the highest speeds.

### Slew rate exceeds 1000V/μsec

This current-boosted amplifier features a slew rate in excess of 1000V/μsec, a full-power bandwidth of 7.5 MHz, and a 3-dB point of 14 MHz. **Fig 4b** shows the circuit driving a 10V pulse into a 50Ω load. Trace A is the input, and trace B is the output. Slew and settling characteristics are quick and clean, and pulse fidelity approaches the quality of the input pulse generator. Note that this circuit relies on summing action, and you can't use it in the noninverting mode.

An often-needed type of voltage-gain stage is one that allows the output to swing very near the supply rails. **Fig 5a** utilizes the resistive nature of the complementary outputs of CMOS logic inverters to make such a stage.

Although using CMOS inverters in such an application might seem unusual, it's a simple, inexpensive way to extend an amplifier's output swing to the supply rails. This circuit is particularly useful in 5V-powered analog systems, where improvements in available output swing are desirable to maximize signal-processing range.

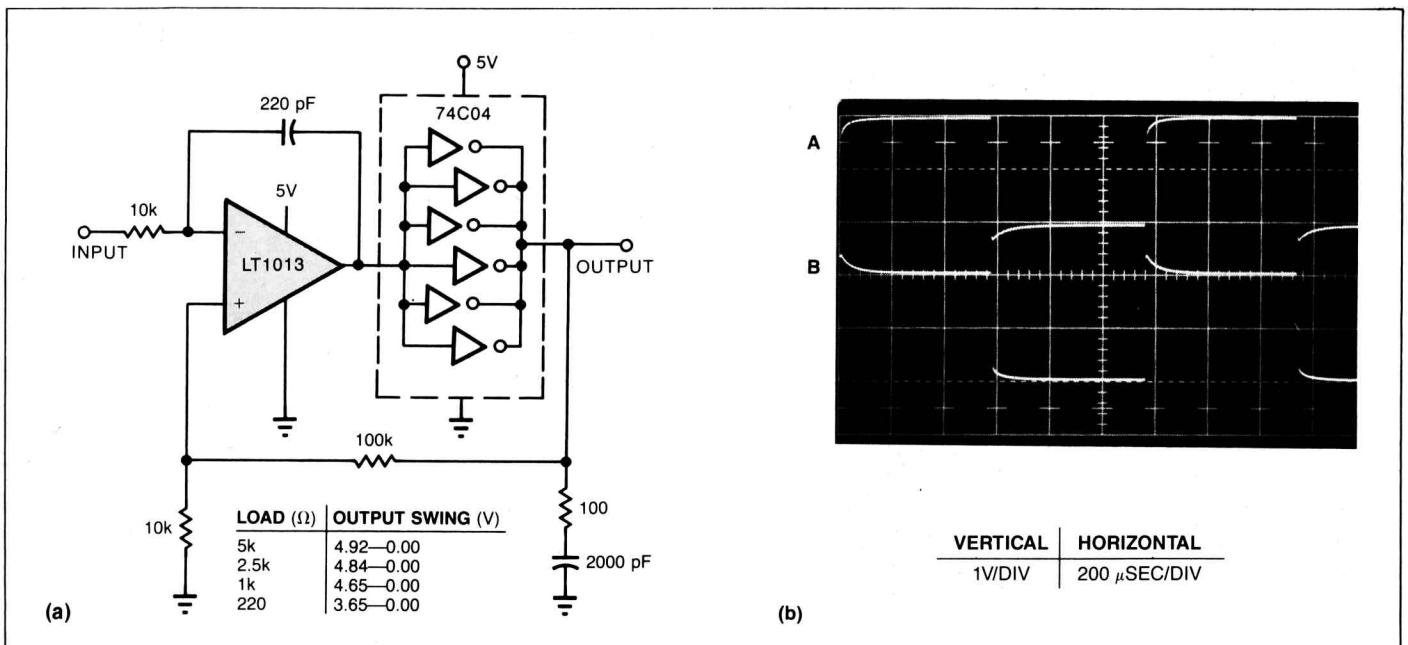



***Fig 5—This unusual circuit employs paralleled CMOS*** *logic inverters operating in their linear region. The design is a simple, inexpensive way to extend an op amp's output swing to the supply rails. Note that, in* ***b****, the op amp's output (trace B) servos around the inverter's switching threshold and that the inverter's output (trace A) swing is quite close to the supply rails.*

*An often-needed form of voltage gain stage is one that allows the output to swing very near the supply rails.*

The paralleled logic inverters are within the LT1013's feedback loop. The paralleling drops output resistance, aiding swing capability. The inversion in the loop requires that the feedback connection go to the amplifier's positive input. An RC damper eliminates oscillation in the inverter stage, which has a high gain-bandwidth product when running in its linear region.

Local capacitive feedback at the amplifier provides loop compensation. The table in **Fig 5a** shows that the output swing is quite close to the positive rail, particularly at loads below several milliamperes. In a servo action, the LT1013's output (trace A in **Fig 5b**) swings around the 74C04's switching threshold (about half the supply voltage) as it controls the circuit's output (trace B). This servo technique allows the amplifier to operate well within its output-swing range while controlling a circuit output with nearly rail-to-rail capability.

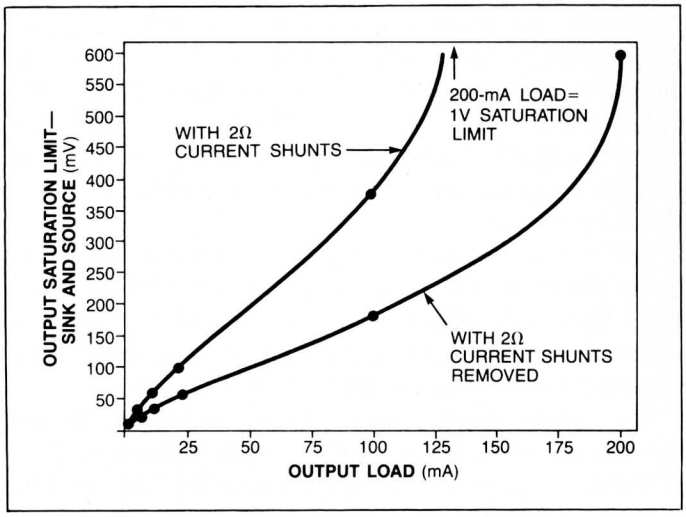



***Fig 7—Removing the current shunts from Fig 6's circuit*** *lowers the circuit's saturation losses, but obviously eliminates short-circuit protection as well.*

### Bipolar stage lowers saturation losses

The configuration in **Fig 6** is similar to **Fig 5a**'s circuit except that the CMOS inverters drive a bipolar output stage to obtain extremely low saturation losses. **Fig 7** plots the circuit's saturation characteristics. If you remove the current-limit circuitry, losses are lowest; however, the output transistors won't tolerate output shorts.

**Fig 8a** is another rail-to-rail output stage, but this circuit features higher output-current and -voltage capability. The stage's voltage gain and low saturation losses allow it to swing nearly to the rails while supplying current gain.

$Q_3$ and $Q_4$, driven by the op amp, provide complementary voltage gain to output transistors $Q_5$ and $Q_6$. In most amplifiers, the output transistors are configured

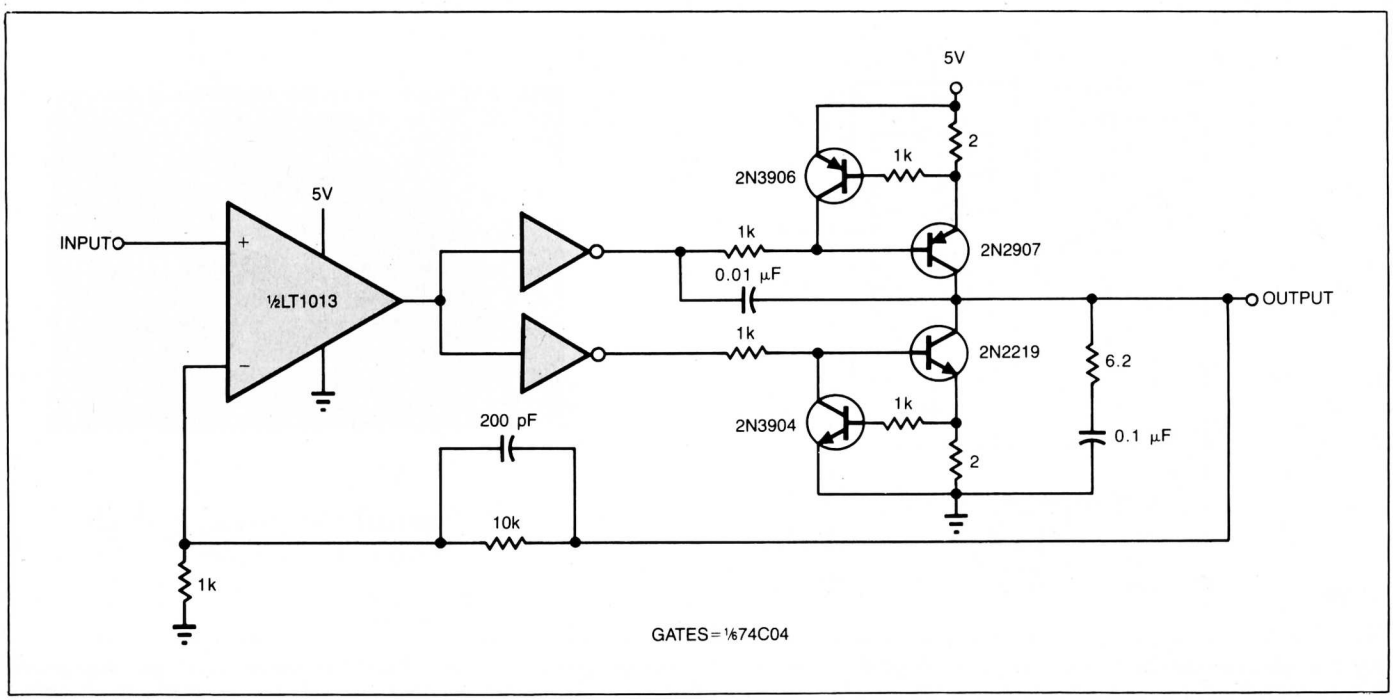
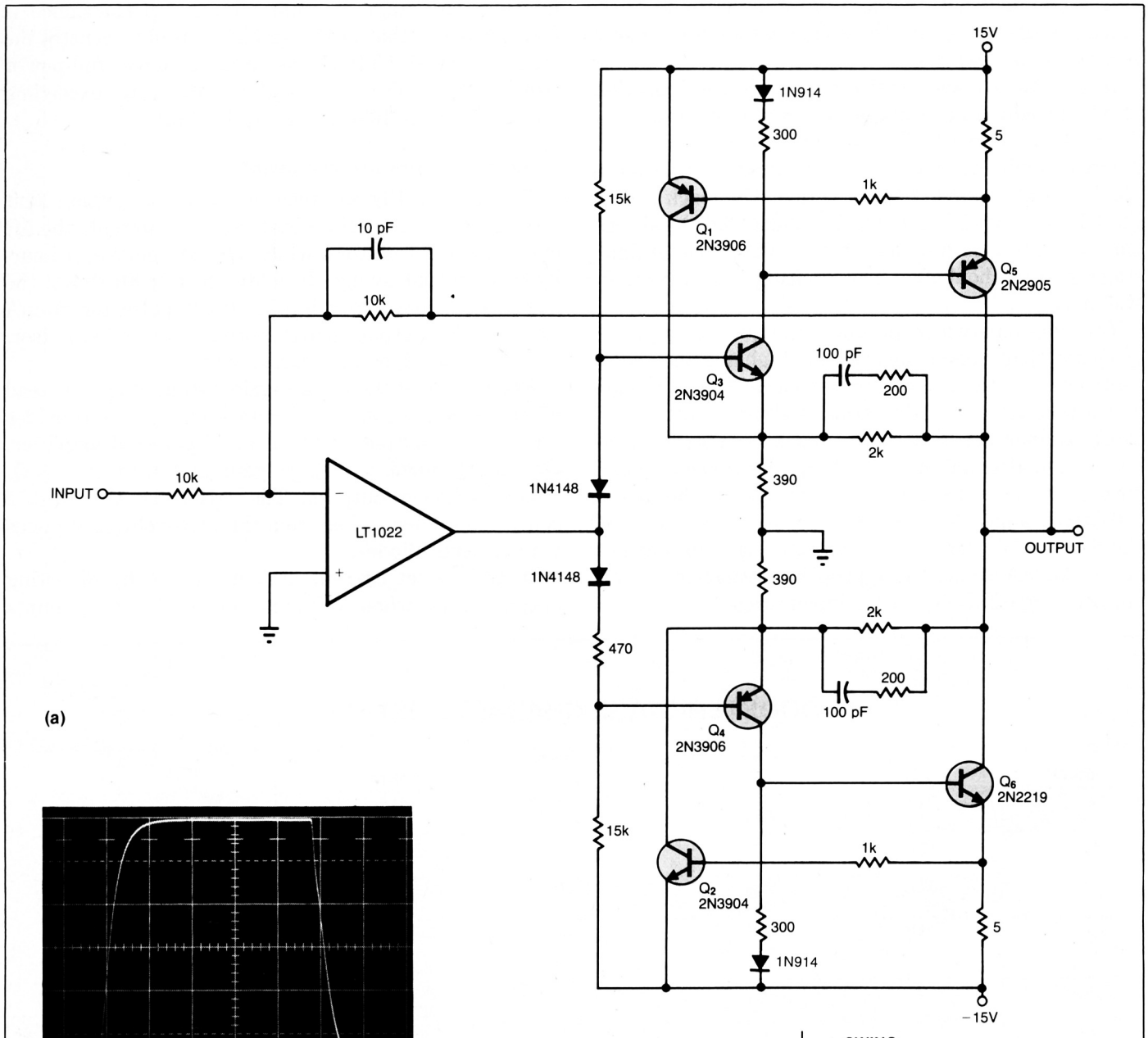



***Fig 6—This circuit is similar to Fig 5a's*** *except that the CMOS inverters drive a bipolar output stage to obtain low saturation losses.*




(a)



| VERTICAL | HORIZONTAL |
|---|---|
| 5V/DIV | 1 μSEC/DIV |

(b)

| OUTPUT CURRENT | ± SWING SATURATION LIMIT |
|---|---|
| 100 μA | 100 mV |
| 1 mA | 160 mV |
| 10 mA | 300 mV |
| 100 mA | 600 mV (150 mV WITH CURRENT LIMIT REMOVED) |

***Fig 8—This rail-to-rail output stage*** *features higher output-current and -voltage capability than the one in* ***Fig 5a.*** *In response to a bipolar input pulse* ***(b),*** *the circuit swings nearly to the supply rails, exhibiting clean dynamics and good slew rate.*

*Obtaining bipolar output from a transformer-based voltage booster requires some form of dc-polarity restoration at the output.*

as emitter followers, furnishing current gain. Their $V_{BE}$ drop, combined with voltage-swing limitations of the driving stage, introduce the swing restrictions characteristic of such stages.

$Q_5$ and $Q_6$ are in a common-emitter configuration, providing additional voltage gain and eliminating $V_{BE}$ drops as a concern. The voltage inversion of these devices combines with the drive-stage inversion to yield overall noninverting operation. Feedback goes to the LT1022's negative input. The 2-kΩ/390Ω local feedback loop associated with each side of the booster limits stage gain to about five. This limiting is necessary for stability.

The gain-bandwidth product available through the $Q_3/Q_5$ and $Q_4/Q_6$ connections is quite high and not readily controllable. The local feedback reduces the gain-bandwidth product, promoting stage stability. The 100-pF/200Ω damper across each feedback resistor provides heavy gain attenuation at very high frequencies, eliminating parasitic local-loop oscillations in the 50- to 100-MHz range. $Q_1$ and $Q_2$, sensing across the 5Ω shunts, furnish 125-mA current limiting. Current flow above 125 mA causes the appropriate transistor to turn on, shutting off the $Q_3$ or $Q_4$ driver stage.

Even with the feedback-enforced gain-bandwidth limiting, the stage is quite fast. AC performance is comparable to that of the amplifier used to control the stage. Using an LT1022, the circuit achieves full-power bandwidth of 600 kHz and a slew rate exceeding 23V/μsec under 100-mA output loading.

### Current sensors are removable

The table in **Fig 8a** gives the swing saturation limit for a given output. Note that, at high current, the 5Ω current-sense resistors, which you can remove, primarily limit output swing. In addition, **Fig 8b** shows the circuit's response to a bipolar input pulse for 25-mA loading. The output swings nearly to the rails, is fast, and has clean dynamic characteristics.

**Fig 9a** is another voltage-gain output stage. Instead of minimizing saturation losses, however, it provides high-voltage outputs from a ±15V-powered amplifier. $Q_1$ and $Q_2$ furnish voltage gain and feed the $Q_3/Q_4$ emitter-follower outputs. The ±15V for the LT1055 control amplifier comes from the high-voltage supplies via the zener diodes.

$Q_5$ and $Q_6$ set current limit at 25 mA by diverting output drive when voltages across the 27Ω shunts

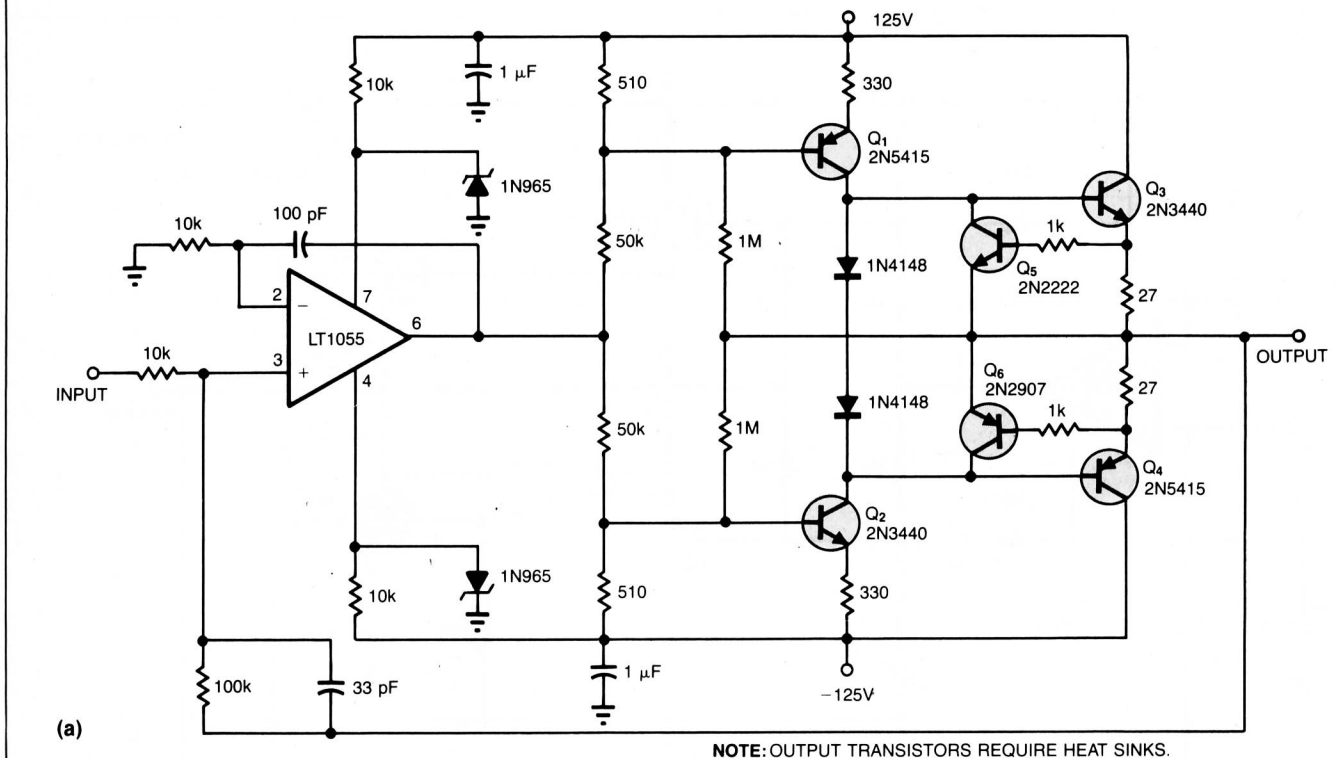
## BOOSTER-STAGE CHARACTERISTICS

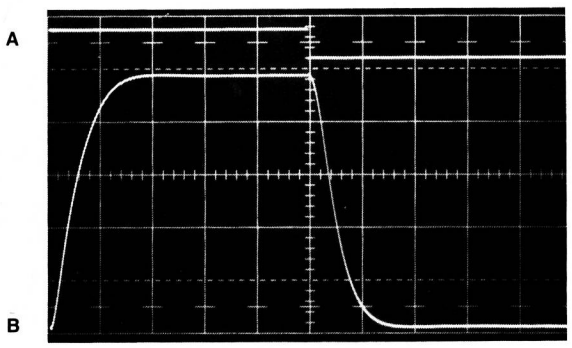
| FIGURE | VOLTAGE GAIN | CURRENT GAIN | FULL-POWER BANDWIDTH | COMMENTS |
|---|---|---|---|---|
| 1a | NO | YES 150 mA | 600 kHz | SIMPLE, EASY. |
| 1b | NO | YES 150 mA | 1.5 MHz | SIMPLE, EASY. |
| 3 | NO | YES 5A | 100 kHz | |
| 4a | NO | YES 200 mA | 7.5 MHz | FEEDFORWARD TECHNIQUE GIVES HIGH BANDWIDTH. SLEW RATE IS GREATER THAN 1000V/μSEC. INVERTING OPERATION ONLY. |
| 5a | YES | NO | DEPENDS ON OP AMP | SIMPLE STAGE ALLOWS WIDE SWING, ALMOST TO RAILS. |
| 8a | YES | YES 125 mA | 600 kHz | HIGH-CURRENT, NEARLY RAIL-TO-RAIL SWING CAPABILITY. |
| 9a | YES ±120V | YES 25 mA | 15 kHz | GOOD, GENERAL-PURPOSE HIGH-VOLTAGE STAGE. |
| 10a | YES ±120V | YES 25 mA | 12 kHz | ALMOST-INDESTRUCTIBLE OUTPUT. |
| 11a | YES 1000V | NO | 60 Hz | HIGH-VOLTAGE OUTPUT; NO EXTERNAL HIGH-VOLTAGE SUPPLIES REQUIRED. LIMITED BANDWIDTH WITH ASYMMETRIC SLEWING. POSITIVE OUTPUTS ONLY. |
| 12a | YES ±100V | YES 150 mA | 150 Hz | HIGH-VOLTAGE OUTPUTS; NO EXTERNAL HIGH-VOLTAGE SUPPLIES REQUIRED. LIMITED BANDWIDTH. FULL BIPOLAR OUTPUT. |

become too high. The local 1-MΩ/50-kΩ feedback pairs set stage gain at 20, allowing the LT1055, supplying by ±10V, to effect a full ±120V output swing. As in **Fig 8a,** the local feedback reduces the stage's gain-bandwidth product, making dynamic control easier.

You can easily provide frequency compensation for this stage because only $Q_1$ and $Q_2$ contribute voltage gain. In addition, the high-voltage transistors have large junctions, resulting in low $f_T$s, and need no special high-frequency rolloff precautions. Frequency compensation comes from rolling off the LT1055 with the local 100-pF/10-kΩ pair. The 33-pF capacitor in the feedback peaks the output's edge response and isn't required for stability.

Because the stage inverts, feedback goes to the LT1055's positive input. Full-power bandwidth is 15 kHz, and slew limit is about 20V/μsec. As shown, the circuit operates in inverting mode, though you can achieve noninverting operation by exchanging the input and ground assignments at the LT1055's input. Under




(b)

| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 50V/DIV | 10 μSEC/DIV |
| B | 50V/DIV (INVERTED) | 10 μSEC/DIV |

***Fig 9—This design (a) provides high-voltage outputs*** *from a circuit containing a ±15V-powered op amp. Applying a ±12V pulse (trace A) (b), results in the cleanly damped, 240V peak-to-peak output pulse (trace B).*

*A parallel-path approach allows very broadband performance without sacrificing the dc stability of the op amp.*

noninverting conditions, you must observe the LT1055's input common-mode-voltage limits and set the minimum noninverting gain at 11.

If you require overcompensation, increasing the 100-pF capacitor's value is preferable to increasing the 33-pF loop-feedback capacitor. Retaining the loop-feedback capacitor prevents excessive high-voltage energy from coupling to the LT1055's inputs during fast slewing. If you must increase the feedback capacitor, you should clamp the summing point with diodes to ground or to the LT1055's supply terminals. **Fig 9b** shows the circuit's response to a ±12V input pulse (trace A). The output (trace B) responds with a cleanly damped, 240V p-p pulse.

**Fig 10a** is a similar stage, except that it replaces **Fig 9a**'s output transistors with vacuum tubes. Most of this stage is conceptually identical to **Fig 9a,** but minor changes are necessary to get the vacuum tubes' output to swing negatively. Replacing **Fig 9a**'s npn emitter follower with a cathode follower ($V_{1A}$) readily achieves a positive swing. The circuit needs the transistor inverter ($Q_3$) because our thermionic friends have no equiva-

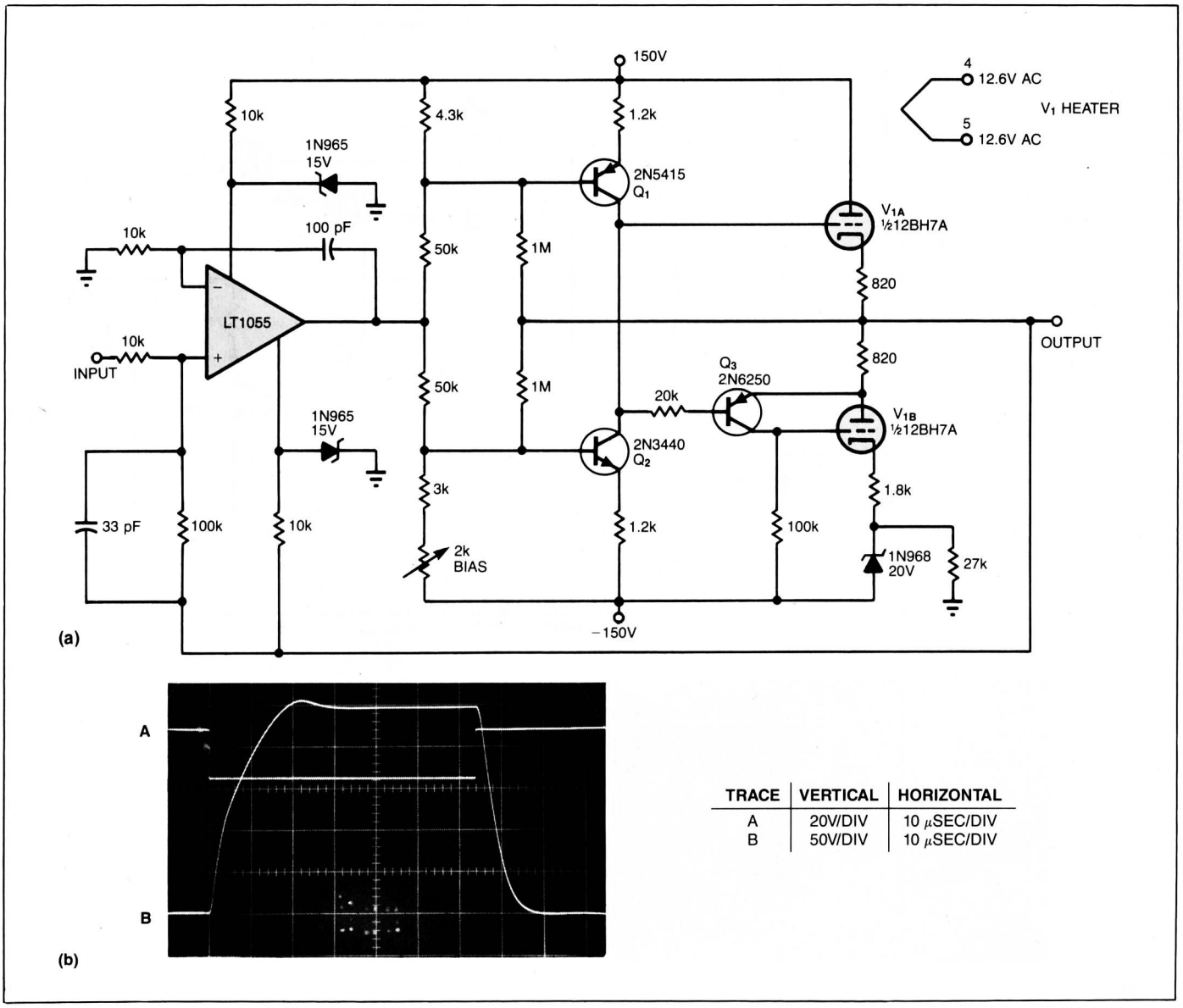
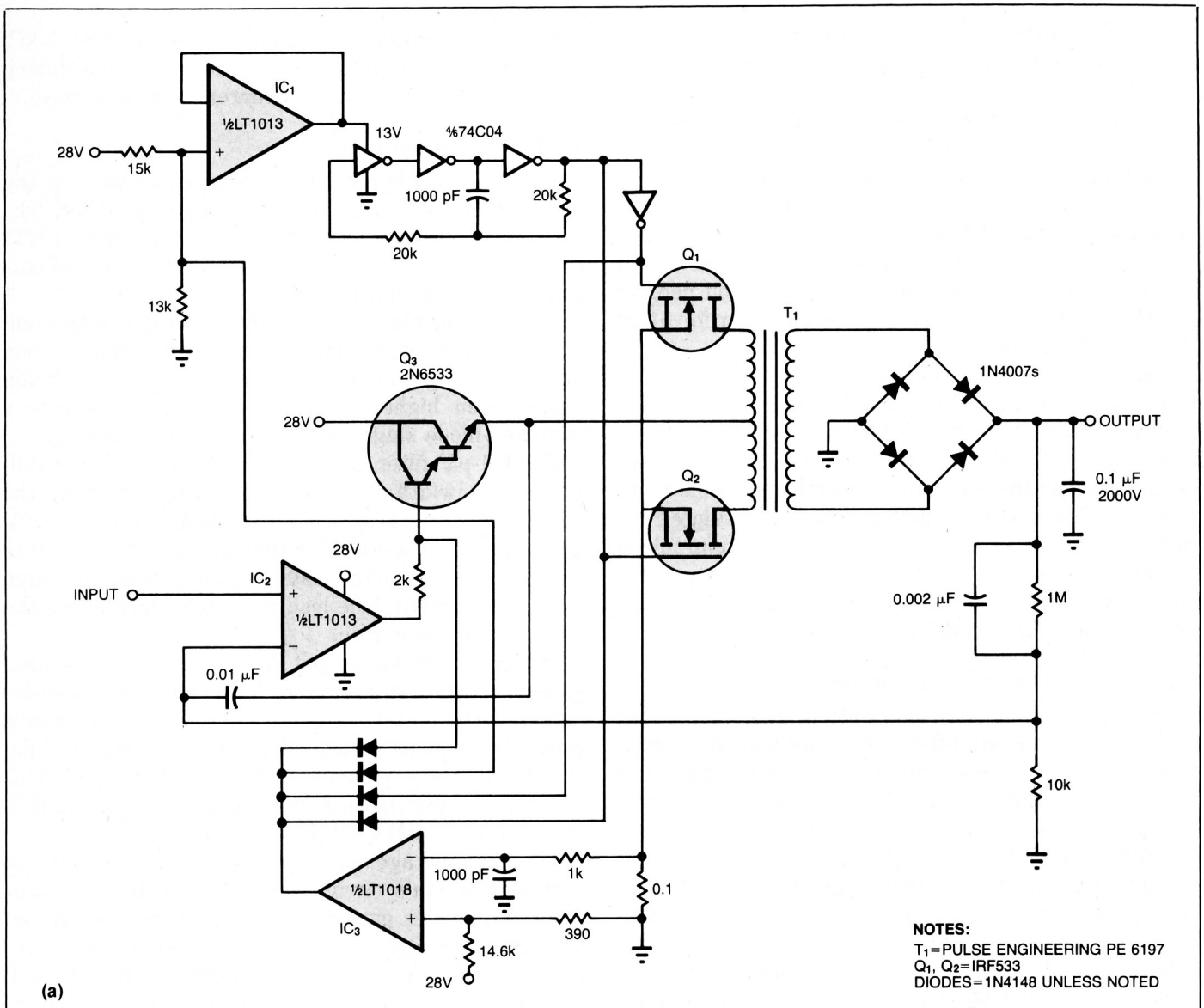
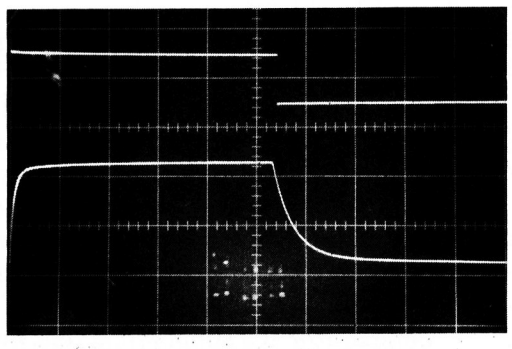



***Fig 10—By replacing Fig 9a's transistors with vacuum tubes (a),*** *you can achieve a rugged and very forgiving op-amp booster with very high-voltage capability. Note that although the circuit's response to a bipolar input is clean and sharp, the stage's asymmetric gain-bandwidth product produces different responses to the leading and trailing edges of the input* ***(b).***




| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 10V/DIV | 5 mSEC/DIV |
| B | 500V/DIV | 5 mSEC/DIV |

***Fig 11—If you need only unipolar outputs,*** *this circuit provides 1000V output swings (for a 10V input), supplies 15W, and requires no separate high-voltage supply—it generates its own high voltage. In* ***b,*** *note that the slewing is faster on the leading edge than the trailing edge of the output pulse (trace B) because the stage cannot sink current. The load resistance determines the falling edge's slew rate.*

*The amount of skew is both load and signal-frequency dependent and isn't readily compensated.*

lent to pnp transistors. Zener biasing of $V_{1B}$'s cathode allows $Q_3$'s swing to cut off the tube, a depletion-mode device.

Without correction, the dc-biasing asymmetry, caused by the $Q_3$ and $V_{1B}$ configuration, will force the LT1055 to bias well away from 0V. Tolerance stack-up could cause saturation limiting in the LT1055's output, reducing overall available swing. Skewing the stage's bias string with the potentiometer adjustment avoids this reduction. To make this adjustment, you need to ground the input and trim the potentiometer for 0V at the LT1055's output.

**Fig 10a**'s full-power bandwidth is 12 kHz, and its slew rate is about 12V/μsec. **Fig 10b** shows the circuit's response to a bipolar input (trace A). The output responds cleanly, although the slew and settling characteristics reflect the stage's asymmetric gain-bandwidth product. This stage's output is extremely rugged because of the inherent forgiving nature of vacuum tubes. It needs no special short-circuit protection, and the output will survive shorts to voltages many times the value of the ±150V supplies.

### Gain stage has a unipolar output

**Fig 11a** shows a unipolar output gain stage that swings 1000V and supplies 15W. Only unipolar operation is possible because the step-up transformer can't pass dc-polarity information. This booster stage has the highly desirable property of operating from a single, low-voltage supply. It doesn't require a separate high-voltage supply; instead, a switching converter (which is an integral part of the gain stage) directly generates the high voltage.

$IC_2$'s output drives $Q_3$, forcing current into $T_1$. MOSFETs $Q_1$ and $Q_2$, which receive complementary drive from the 74C04-based square-wave oscillator, chop $T_1$'s primary current. $IC_1$ supplies power to the oscillator. $T_1$ provides voltage step-up. $T_1$'s rectified and filtered output is the booster stage's output.

The 1-MΩ/10-kΩ divider furnishes feedback to $IC_2$, closing a loop around it. The 0.01-μF capacitor from $Q_3$'s emitter to $IC_2$'s negative input provides loop stability, and the 0.002-μF unit trims step-response damping.

Comparator $IC_3$ provides short-circuit limiting. Current from $Q_1$ and $Q_2$ passes through the 0.1Ω shunt, which develops the error signal for $IC_3$. Abnormal output currents cause the shunt voltage to rise, tripping $IC_3$'s output low. This tripping simultaneously removes drive from $Q_3$, $Q_1$, and $Q_2$'s gates as well as the oscillator, resulting in output shutdown. The 1-kΩ/1000-pF filter ensures that $IC_3$ does not trip during normal operation because of current spikes or noise.

### FETs work down to 0V

$IC_2$ supplies whatever drive is required to close the loop, regardless of the output voltage called for. The low, resistive-saturation losses of the VMOS FETs combined with $IC_2$'s servo action allows controlled outputs all the way down to 0V.

Substituting higher power devices for $Q_1$ and $Q_2$ along with a larger transformer allows more output power, although dissipation in $Q_3$ will become excessive. If you desire even higher power, you should substitute a switched-mode stage for $Q_3$ to maintain efficiency.

The 0.1-μF filter capacitor at the output limits full-power bandwidth to about 60 Hz. **Fig 11b** shows the circuit's dynamic response at full load. Trace A, a 10V input, produces a 1000V output in trace B. Note that slewing is faster on the leading edge because the stage can't sink current. The load resistance determines the falling edge's slew rate.

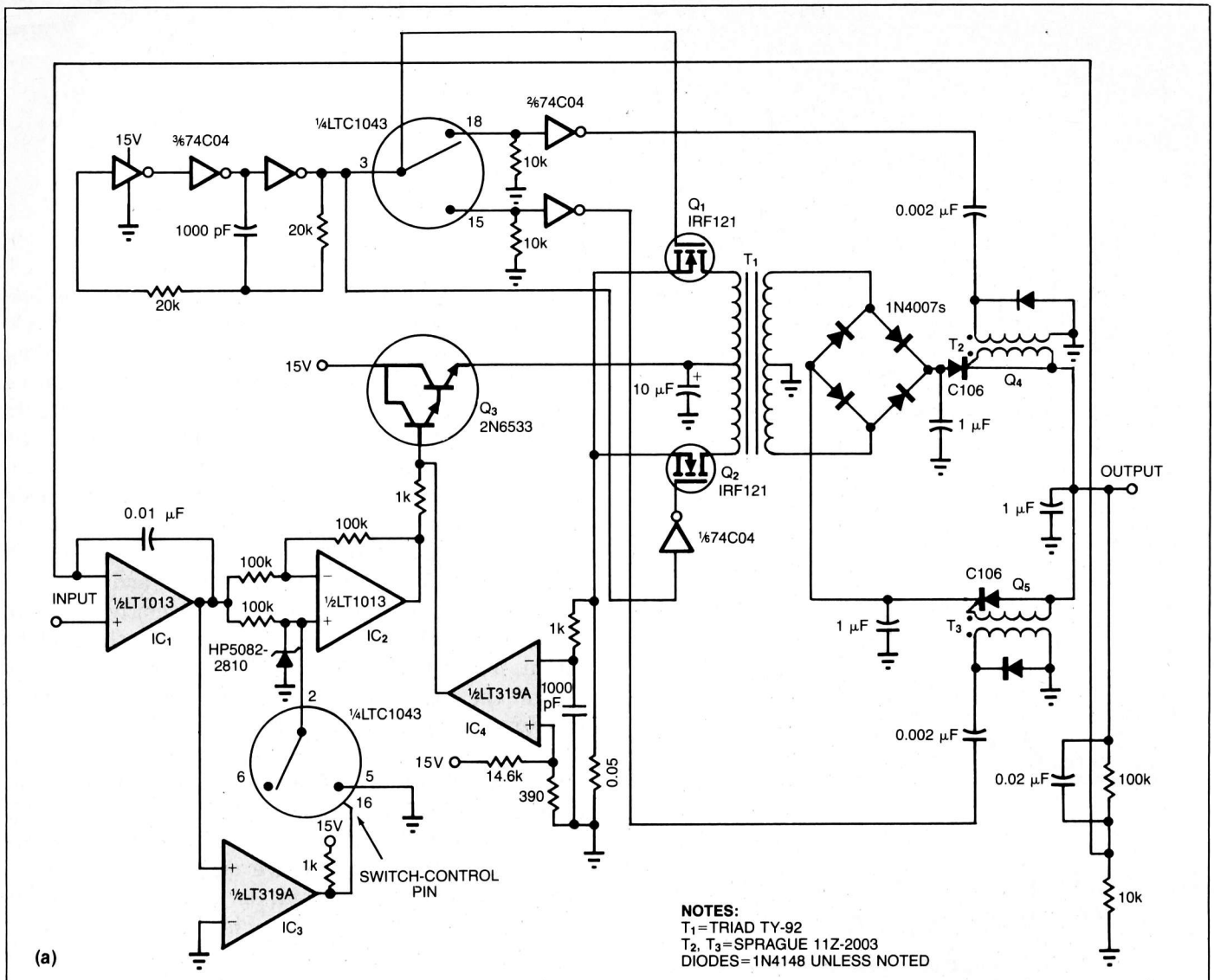
Obtaining bipolar output from a transformer-based voltage booster requires some form of dc-polarity restoration at the output. **Fig 12a**'s ±15V-powered circuit provides this restoration, using synchronous demodulation to preserve polarity in its ±100V output. This booster features 150-mA current output, 150-Hz full-power output, and 0.1V/μsec slew rate.

The high-voltage output's generation is similar to that in **Fig 11a**'s circuit. The 74C04-based oscillator furnishes bipolar gate drive to VMOS devices $Q_1$ and $Q_2$, which chop $Q_3$'s output into $T_1$, a step-up transformer. In this design, however, a synchronously switched, absolute-value amplifier sits between servo amplifier $IC_1$ and $Q_3$'s drive point.

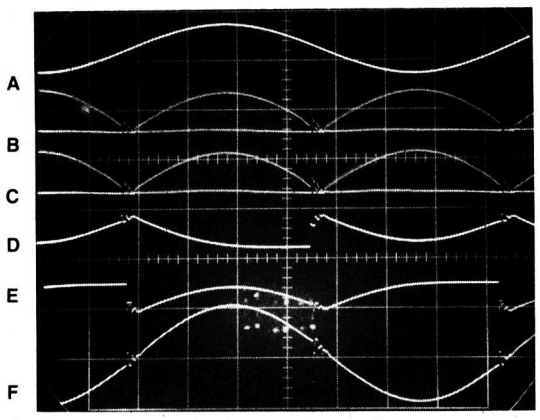
Input-signal polarity information, derived from $IC_1$'s output, causes comparator $IC_3$ to switch the LTC1043 section located at $IC_2$'s positive input. In this circuit, $IC_2$'s output is the positive absolute value of $IC_1$'s input signal. A second, synchronously switched, LTC1043 section gates the oscillator's pulses to the appropriate SCR's trigger transformer at the output. Positive inputs cause pin 2 to connect to pin 6, as well as pin 3 to pin 18, in the LTC1043.

Comparator $IC_4$ supplies current limiting in identical fashion to **Fig 11a**'s scheme. Frequency compensation is also similar. A 0.01-μF capacitor at $IC_1$ provides loop stability, and the 0.02-μF feedback unit sets damping.

$IC_2$, acting as a unity-gain follower, passes $IC_1$'s

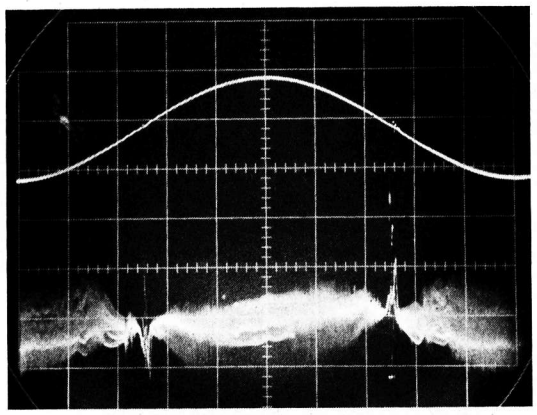



(a)




| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 10V/DIV | 5 mSEC/DIV |
| B | 20V/DIV | 5 mSEC/DIV |
| C | 20V/DIV | 5 mSEC/DIV |
| D | 100V/DIV | 5 mSEC/DIV |
| E | 100V/DIV | 5 mSEC/DIV |
| F | 50V/DIV | 5 mSEC/DIV |

(b)




| TRACE | VERTICAL | HORIZONTAL |
|---|---|---|
| A | 100V/DIV | 10 mSEC/DIV |
| B | 0.2V/DIV (1% DISTORTION) | 10 mSEC/DIV |

(c)

***Fig 12—Obtaining bipolar output from a transformer-based*** *voltage booster requires dc-polarity restoration. This circuit* ***(a)*** *uses synchronous demodulation to preserve polarity in its ±100V output. Except for some distortion at the zero crossover caused by phase skewing between the SCR switching and the carrier-borne signal* ***(b),*** *trace F shows an amplified, reconstructed version of the sine-wave input (trace A). Traces B and C are the FETs' drain waveform; traces D and E are the full-wave bridge's negative and positive outputs. At a full load of ±100V and 150 mA peak, the circuit produces the distortion products in trace B* ***(c).*** *You can see residual, high-frequency-carrier components, and the zero-point SCR switching causes the sharp peaks.*

output directly and drives $Q_3$. Simultaneously, oscillator pulses conduct through an inverter via LTC1043 pin 18. The inverter drives trigger transformer $T_2$, turning $Q_4$ on. $Q_4$, biased from the full-wave bridge's positive point, supplies positive polarity voltage to the output.

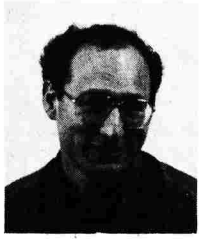
Negative inputs cause the LTC1043 switch positions to reverse. $IC_2$, functioning as an inverter, again supplies $Q_3$ with positive voltage drive. The Schottky diode at $IC_2$ prevents the LTC1043 from seeing transient negative voltages. Oscillator pulses go to SCR $Q_5$ via LTC1043 pin 15, its associated inverter, and $T_3$.

$Q_5$ connects the full-wave bridge's negative point to the output. Both SCRs, tied together, form the circuit's output. The 100-kΩ/10-kΩ divider supplies feedback to $IC_1$ in the conventional manner. The synchronous switching preserves polarity information from the stage's output, permitting bipolar operation.

**Fig 12b** shows waveforms for a sine-wave input. Trace A is $IC_1$'s input. Traces B and C are $Q_1$ and $Q_2$'s drain waveforms. Traces D and E are the full-wave bridge's negative and positive outputs, respectively. Trace F, the circuit output, is an amplified, reconstructed version of $IC_1$'s input. Phase skewing between the SCR switching and the carrier-borne signal causes some distortion at the zero crossover. The amount of skew is both load and signal-frequency dependent and is not readily compensated.

**Fig 12c** shows distortion products (trace B) at 10 Hz output (trace A) at full load (±100V at 150 mA peak). Residual, high-frequency-carrier components are clearly present, and the zero-point SCR switching causes the sharp peaks. RMS distortion measures 1% at 10 Hz, rising to 6% at 100 Hz. **EDN**

## Author's biography



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Article Interest Quotient (Circle One)
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