6.0 Appendices

A1.0 POWER SUPPLY DESIGN

A1.1 Introduction

One of the nebulous areas of power IC data sheets involves the interpretation of "absolute maximum ratings" as opposed to "operating conditions." The fact that parameters are specified at an operating voltage quite a few volts below the absolute maximum is not nearly so important in "garden variety" op amps as in power amps — because a key spec of any power amplifier is how much power it can deliver, a spec that is a strong function of the supply. Indeed P_O is approximately proportional to the square of supply voltage. Since many audio ICs are powered from a step down transformer off the 120V_{AC} line, the "absolute maximum voltage" is an attempt to spec the highest value the supply might ever reach under power company overvoltages, transformer tolerances, etc. This spec says the IC will not die if taken to its "absolute maximum rating." Operating voltage, on the other hand, should be approximately what a nominal supply will sag under load at normal power company voltages. Some audio amplifiers are improperly specified at their "absolute maximum voltages" in order to give the illusion of large output power capability. However, since few customers regulate the supply voltage in their applications of audio ICs, this sort of "specsmanship" can only be termed deceptive.

A1.2 General

This section presents supply and filter design methods and aids for half-wave, full-wave center tap, and bridge rectifier power supplies. The treatment is sufficiently detailed to allow even those unfamiliar with power supply design to specify filters, rectifier diodes and transformers for single-phase supplies. A general treatment referring to Figure A1.1 is given, followed by a design example. No attempt is made to cover multiphase circuits or voltage multipliers. For maximum applicability a regulator is included, but may be omitted where required.

A1.3 Load Requirements

The voltage, current, and ripple requirements of the load must be fully described prior to filter and supply design. Actually, so far as the filter and supply are concerned, the load requirements are those at the regulator input. (See Figure A1.1.) Therefore, V_{IN} and I_{IN} become the governing conditions, where:

$I_{IN} = I_O + I_Q$, output current plus regulator quiescent current

$I_{IN(MAX)} \approx I_{O(MAX)}$, full-load operating current

$I_{IN(MIN)} \leq I_Q$, no-load or minimum operating current; could be near zero

$V_{IN(PK)} = V_M$, maximum permissible instantaneous no-load filter output voltage equal to peak value of transformer secondary voltage at highest design line voltage V_{PRI}; limited by absolute maximum regulator input voltage

$V_{IN} > V_O$, nominal DC voltage input to the regulator, usually 2 to 15V higher than V_O

$V_{IN(MIN)} \approx V_O + 2V$, minimum instantaneous full-load filter output voltage including ripple voltage; limited by minimum regulator input voltage to insure satisfactory regulation ($V_O + V_{dropout}$) or minimum regulator input voltage to allow regulator start-up under full load or upon removal of a load short circuit

r_f RMS ripple factor at filter output expressed as a percentage of V_{IN}; limited by maximum permissible ripple at load as modified by the ripple rejection characteristics of the regulator

A1.4 Filter Selection, Capacitor or Inductor-Input

For power supplies using voltage regulators, the filter will most often use capacitor input; therefore, emphasis will be placed upon that type of filter in following discussions. Notable differences between the two types of filters are that the capacitor input filter exhibits:

1. Higher DC output voltage
2. Poorer output voltage regulation with load variation
3. Higher peak to average diode forward currents

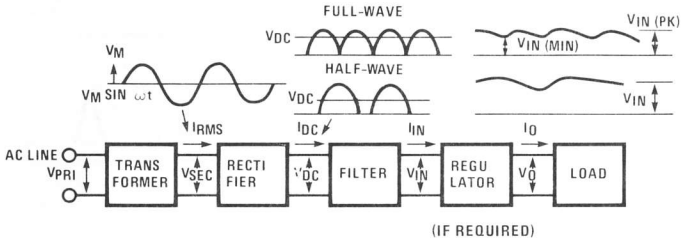
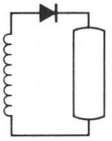
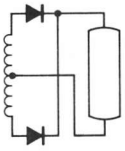
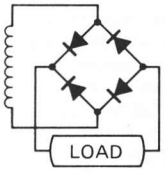
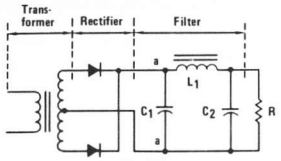


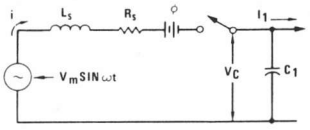
FIGURE A1.1 Power Supply Block Diagram, General Case

TABLE A1.1 Summary of Significant Rectifier Circuit Characteristics, Single Phase Circuits
Capacitive Data is for $\omega C R_L = 100$ & $R_S/R_L = 2\%$ (higher values) and for $\omega C R_L = 10$ & $R_S/R_L = 10\%$ (lower values)

	Single Phase Half Wave			Single Phase Full Wave Center Tap			Single Phase Full Wave Bridge		
Rectifier Circuit Connection									
Voltage Waveshape to Load of Filter									
CHARACTERISTIC LOAD	R	L	C	R	L	C	R	L	C
Average Diode Current $I_{F(AVG)}/I_{O(DC)}$	1	1	1	0.5	0.5	0.5	0.5	0.5	0.5
Peak Diode Current $I_{FM}/I_{F(AVG)}$	3.14	-	8 5.2	3.14	2	10 6.2	3.14	2	10 6.2
Diode Current Form Factor, $F = I_{F(RMS)}/I_{F(AVG)}$	1.57	-	2.7 2	1.57	1.41	3 2.2	1.57	1.41	3 2.2
RMS Diode Current $I_{F(RMS)}/I_{O(DC)}$	1.57	-	2.7 2	0.785	0.707	1.35 1.1	0.785	0.707	1.35 1.1
RMS Input Voltage per Transformer Leg $V_{SEC}/V_{IN(DC)}$	2.22	2.22	0.707	1.11	1.11	0.707	1.11	1.11	0.707
Transformer Primary VA Rating VA/P_{DC}	3.49	-	-	1.23	1.11	-	1.23	1.11	-
Transformer Secondary VA Rating VA/P_{DC}	3.49	-	-	1.75	1.57	-	1.23	1.11	-
Total RMS Ripple %	121	-	-	48.2	-	-	48.2	-	-
Rectification Ratio (Conversion Efficiency) %	40.6	-	-	81.2	100	-	81.2	100	-



(a) Actual Circuit

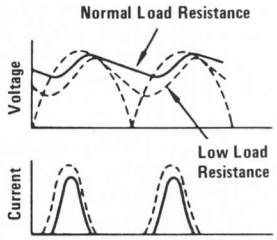


(b) Equivalent Circuit

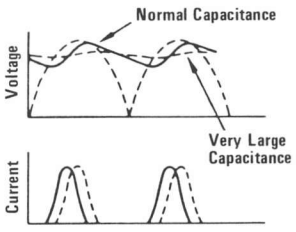
(c) Voltage Across Input Capacitor C_1

(d) Current Through Diodes

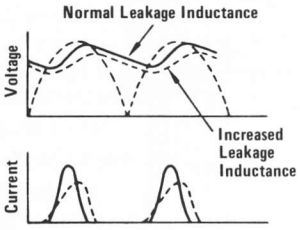
FIGURE A1.2 Actual and Equivalent Circuits of Capacitor-Input Rectifier System, Together with Oscillograms of Voltage and Current for a Typical Operating Condition



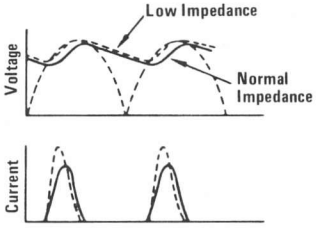
(a) Actual Circuit



(b) Equivalent Circuit



(c) Voltage Across Input Capacitor C_1



(d) Current Through Diodes

FIGURE A1.3 Effects of Circuit Constants and Operating Conditions on Behavior of Rectifier Operated with Capacitor-Input Filter

4. Lower diode PIV rating requirements
5. Very high diode surge current at turn-on
6. Higher peak to average transformer currents

The voltage regulator overcomes disadvantage (2) while semiconductor diodes of moderate price meet most of the peak and surge requirements except in supplies handling many amperes. Still, it may be necessary to balance increased diode and transformer cost against the alternative of a choke-input filter. In power supply designs employing voltage regulators, it is assumed that only moderate filter output regulation and ripple are required. Therefore, a capacitor input filter would exhibit peak currents considerably lower than indicated in the comparison of Table A1.1.

A1.5 Filter Design, Capacitor-Input

Figure A1.2 shows a full-wave, capacitor-input (filter) rectifier system with typical voltage and current waveforms. Note that ripple is inevitable as the capacitor discharges approximately linearly between voltage peaks. Figure A1.3 shows the effects on DC voltage, ripple, and peak diode current under varying conditions of load resistance, input capacitance, series diode and transformer resistance R_S, and transformer leakage inductance. The most practical design procedure for capacitor-input filters is to use the graphs of Figures A1.4-A1.7. Note, however, that these include the effects of diode dynamic resistance within R_S. Diode forward drop is not included, and must be subtracted from the transformer secondary voltage. A good rule of thumb is to subtract 0.7 V from the transformer voltage and assume diode dynamic resistance is insignificant (0.02 Ω at I_F = 1 A, 0.26 Ω at I_F = 100 mA); ordinarily the transformer resistance will overshadow diode dynamic resistance.

Figures A1.4 and A1.5 show the relationship between peak AC input voltage and DC output voltage as a relation to load resistance R_L, series circuit resistance R_S, and filter input capacitance C. Figure A1.4 is for half-wave rectifiers and Figure A1.5 is for full-wave rectifiers. Note that the horizontal axis is labeled in units of $\omega C R_L$ where:

ω = AC line frequency in Hertz x 2π

C = value of input capacitor in Farads

$R_L = V_{IN}/I_{IN} \approx V_O/I_O$, equivalent load resistance in Ohms

R_S = total of diode dynamic resistance, transformer secondary resistance, reflected transformer primary resistance, and any added series surge limiting resistance

The major design trade-off encountered in designing capacitor-input filters is that between achieving good voltage regulation with low ripple and achieving low cost.

Referring to Figures A1.4 and A1.5:

1. Good regulation means $\omega C R_L \approx 10$.
2. Low ripple may mean $\omega C R_L > 40$.
3. High efficiency means $R_S/R_L < 0.02$.
4. Low cost usually means low surge currents and small C.
5. Good transformer utilization means low VA ratings, best with full-wave bridge FWB circuit, followed by full-wave center tap FWCT circuit.

In most cases, a minimum capacitance accomplishing a reasonable full-load to no-load regulation is preferable for low cost. To achieve this, use an intercept with the upper

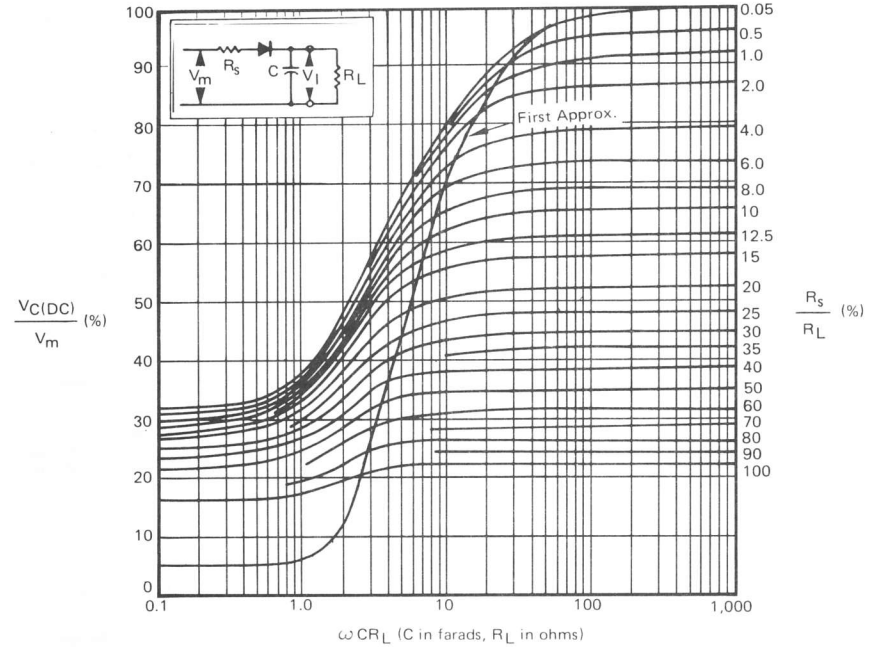


FIGURE A1.4 Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Half-Wave Capacitor-Input Circuits (From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)

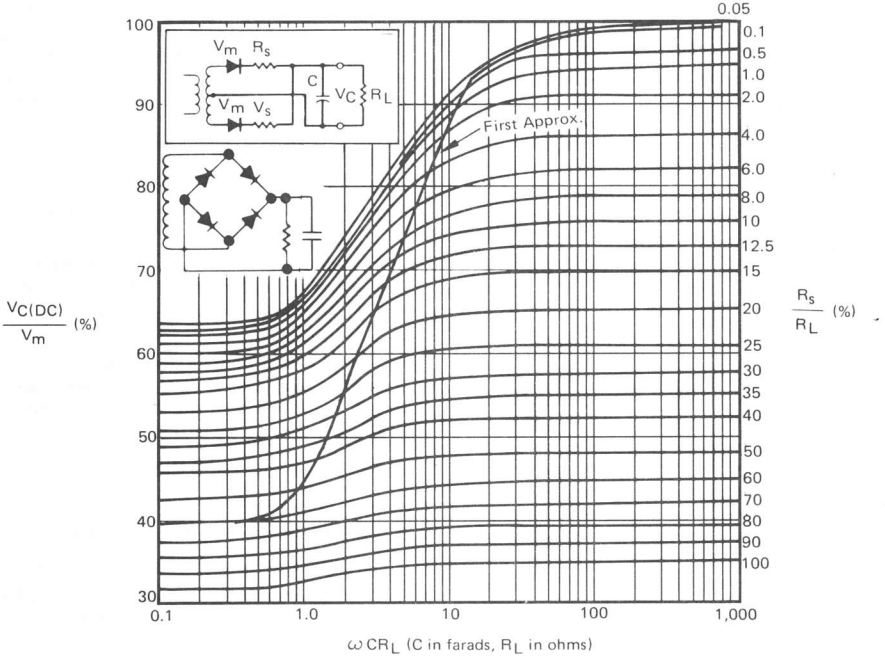


FIGURE A1.5 Relation of Applied Alternating Peak Voltage to Direct Output Voltage in Full-Wave Capacitor-Input Circuits (From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)

knee of the curves in Figures A1.4 and A1.5. Occasionally, a minimum value filter capacitor will not result in a lower cost system. For example, increasing the value of C may allow higher R_S/R_L to result in lower surge and RMS currents, thus allowing lower cost transformers and diodes. Be sure that capacitors used have adequate ripple current ratings.

Design procedure is as follows:

1. Assuming that V_O, I_O, ω, and load ripple factor r_f have been established and an appropriate voltage regulator has been selected, we know or can determine:

   $\omega = 2\pi f = 377$ rad/sec for 60 Hz line

   $r_{f(in)} = r_{f(out)}$ x ripple reduction factor of selected regulator

   $V_{IN(PK)} \leq$ Max V_{IN} for the selected regulator; allow for highest line voltage likely to be encountered

   $I_{IN(MIN)} \approx V_O + 2V$; allow for lowest line voltage

   $V_{IN(DC)}{}^+ = V_{IN}$, usually 2-15V above V_O; if chosen midway between $V_{IN(PK)}$ and $V_{IN(MIN)}$ or slightly below that point, will allow for greatest ripple voltage

   $I_{IN} \approx I_O$ for full load

   $I_{IN(MIN)} = I_Q$ for open load

   $R_L = V_{IN(DC)}/I_{IN}$

   $R_{L(MIN)} = V_{IN(MIN)}/I_{IN}$

2. Set $V_M \leq V_{IN(PK)}$ and calculate $V_{IN(DC)}/V_{IN}$. Enter the graph of Figure A1.4 or A1.5 at the calculated $V_{IN(DC)}/V_M$ to intercept one of the R_S/R_L = constant lines. Either estimate R_S at this time or intercept the curve marked "First Approximation."

3. Drop vertically from the intercept of Step (2) to the horizontal axis and read $\omega C R_L$. Calculate C, allowing for usual commercial tolerance on capacitors of +100, -50%.

   If $V_{IN(DC)}$ is midway between $V_{IN(PK)}$ and $V_{IN(MIN)}$, the supply can present maximum ripple to the regulator. A low value of C is then practical. If $V_{IN(DC)}$ is near $V_{IN(MIN)}$, regulator power dissipation is low and supply efficiency is high; however, ripple must be low, requiring large C.

4. Determine ripple factor r_f from Figure A1.6. Make certain that the ripple voltage does not drop instantaneous V_{IN} below $V_{IN(MIN)}$.

   The ripple factor could determine minimum required C if ripple is the limiting factor instead of voltage regulation. Again, allow for -50% tolerance on the capacitor.

$$V_{ripple(pk)} = \sqrt{2}\,\frac{r_f}{100}\,V_{IN(DC)}$$

A1.6 Diode Specification

Find diode requirements as follows:

1. $I_{F(AVG)} = I_{IN(DC)}$ for half-wave rectification
   $= I_{IN(DC)}/2$ for full-wave rectification

2. Determine peak diode current ratio from Figure A1.7; remember to allow for highest operating line voltage and +100% capacitor tolerance.

   $I_{FM} = I_{FM}/I_{F(AVG)} \times I_{IN(DC)}$ for half-wave
   $= I_{FM}/I_{F(AVG)} \times I_{IN(DC)}/2$ for full-wave

3. Determine diode surge current requirement at turn-on of a fully discharged supply when connected at the peak of the highest expected AC line waveform. Surge current is:

$$I_{SURGE} = \frac{E_M}{R_S + ESR}$$

   where ESR = effective series resistance of capacitor.

4. Find required diode PIV rating from Figure A1.8. Actually, required PIV may be considerably more than the value thus obtained due to noise spikes on the line. See Section A1.9 for details on transient protection. Remember that the PIV for the diodes in the FWB configuration are one half that of diodes as found in FWCT or HW rectifier circuits.

The diodes may now be selected from diode manufacturers' data sheets. If calculated surge current rating or peak current ratings are impractically high, return to Step A1.5(2) and choose a higher R_S/R_L or lower C. Conversely, it may be practical to choose lower R_S/R_L or higher C if diode current ratings can be practically increased without adverse effect on transformer cost; the result will be higher supply efficiency.

A1.7 Transformer Specification

A decision may have been made at Step A1.5(2) as to using half-wave or full-wave rectification. The half-wave circuit is often all that is required for low current regulated supplies; it is rarely used at currents over 1A, as large capacitors and/or high surge currents are dictated. Transformer utilization is also quite low, meaning that higher VA rating is required of the transformer in HW circuits than in FW circuits. (See VA ratings of Table A1.1.)

Half-wave circuits are characterized by low $V_{IN(DC)}/V_M$ ratio, or very large C required (about 4 times that required for FW circuits, high ripple, high peak to average diode and transformer current ratios, and poor transformer utilization). They do, however, require only one diode.

Full-wave circuits are characterized by high $V_{IN(DC)}/V_M$ ratio, low C value required, low ripple, low peak to average diode and transformer current ratios, and good transformer utilization. They do require two diodes in the center-tap version, while the bridge configuration with its very high transformer utilization requires four diodes.

The information necessary to specify the transformer is:

1. Half-wave, full-wave CT or full-wave bridge circuit
2. Secondary V_{RMS} per transformer leg, $(V_M + 0.7^*)/\sqrt{2}$, from Section A1.5
3. Total equivalent secondary resistance including reflected primary resistance from Section A1.5
4. Peak, average, and RMS diode or winding currents from Sections A1.6(1) and -(2), and VA ratings.

*1.4 for full-wave bridge circuit.

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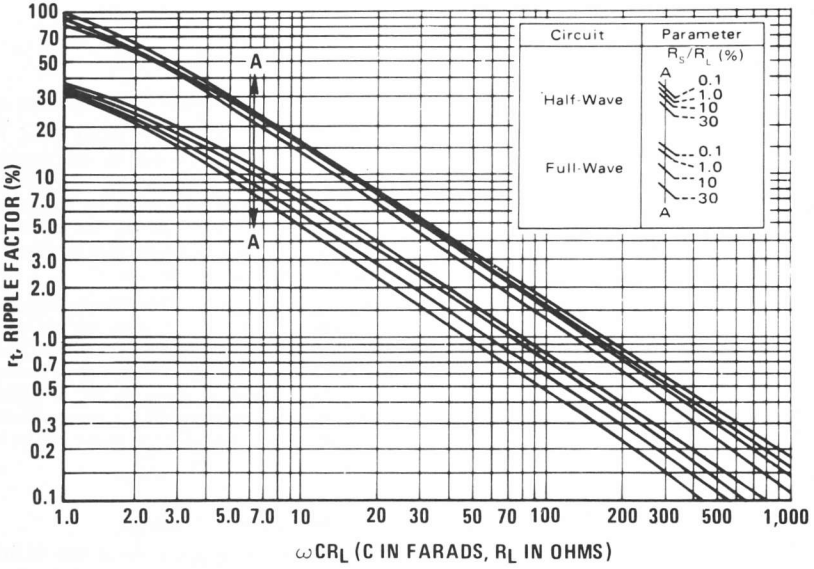


FIGURE A1.6 Root-Mean-Square Ripple Voltage for Capacitor-Input Circuits
(From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)

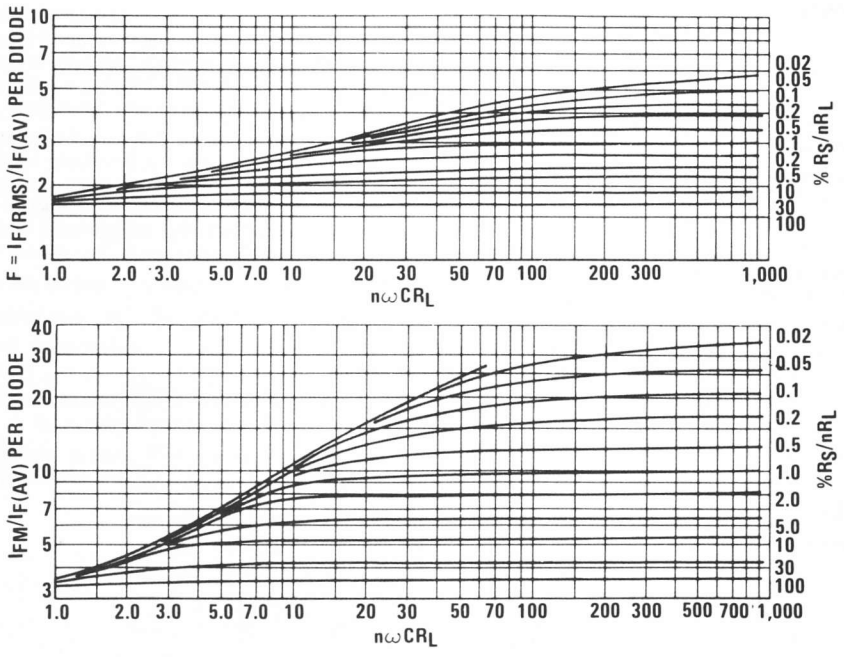


FIGURE A1.7 Relation of RMS and Peak-to-Average Diode Current in Capacitor-Input Circuits
(From O. H. Schade, Proc. IRE, vol. 31, p. 356, 1943.)

Transformer VA rating and secondary current ratings are determined as follows:

		FWB	FWCT	HW
$I_{RMS(SEC)}$	=	$I_{IN(DC)}\,F/\sqrt{2}$	$I_{IN(DC)}\,F/2$	$I_{IN(DC)}\,F$
VA_{SEC}	=	$V_{RMS}\,I_{RMS}$	$2\,V_{RMS}\,I_{RMS}$	$V_{RMS}\,I_{RMS}$
VA_{PRI}	=	VA_{SEC}	$VA_{SEC}/\sqrt{2}$	VA_{SEC}

where: $F = I_{R(RMS)}/I_{IN(DC)}$
= form factor from Figure A1.7
V_{RMS} = secondary RMS voltage per leg

A1.8 Additional Filter Sections

Occasionally, it is desirable to add an additional filter to reduce ripple. When this is done, an LC filter section is cascaded with the single C section filter already designed. If the inductor is of low resistance, the effect on output voltage is small. The additional ripple reduction may be determined from Figure A1.9.

A1.9 Transient Protection

Often the PIV rating of the rectifier diodes must be considerably greater than the minimum value determined from Figure A1.8. This is due to the likely presence of high-voltage transients on the line. These transients may be as high as 400V on a 115V line. The transients are a result of switching inductive loads on the power line. Such loads could be motors, transformers, or could even be caused by SCR lamp dimmers or switching-type voltage regulators, or the reverse recovery transients in rectifying diodes. As the transients appearing on the transformer primary are coupled to the secondary, the rectifier diodes may see rather high peak voltages. A simple method of protecting against these transients is to use diodes with very high PIV. However, high-current diodes with very high PIV ratings can be expensive.

There are several alternate methods of protecting the rectifier diodes. All rely on the existence of some line impedance, primary transformer resistance or secondary circuit resistance. See Figure A1.10 for the system circuit.

The several methods of transient protection rely on shunting the transient around the rectifier diodes to dissipate the transient energy in the series circuit resistance and the protective device. The usual protection methods are:

1. Series resistor at the primary with shunt capacitor across the primary winding – see Figure A1.10

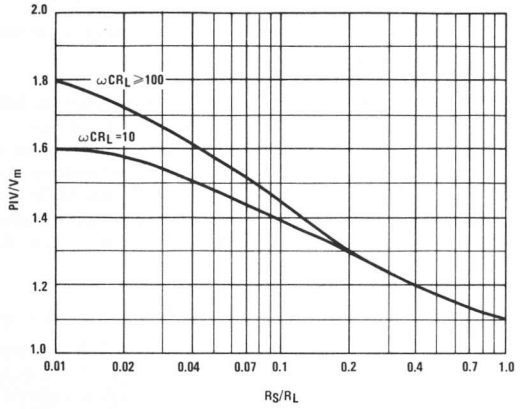


FIGURE A1.8 Ratio of Operating Peak Inverse Voltage to Peak Applied AC for Rectifiers Used in Capacitor-Input, Single-Phase, Filter Circuits

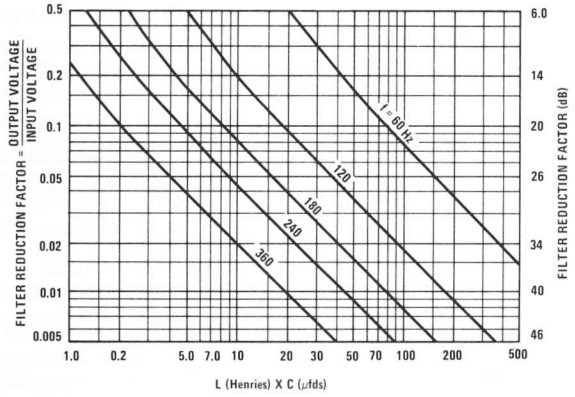


FIGURE A1.9 Reduction in Ripple Voltage Produced by a Single Section Inductance-Capacitance Filter at Various Ripple Frequencies

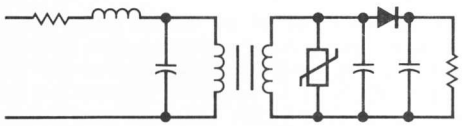
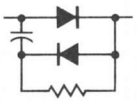


FIGURE A1.10 Transformer/Filter Circuit Showing Placement of Transient Protection Components

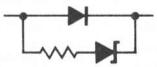
2. Series inductance at the primary, possibly with a shunt capacitor across the primary – see Figure A1.10
3. Shunt capacitor on the secondary – see Figure A1.10
4. Capacitor shunt on the rectifier diode – transient power is thus dissipated in circuit series resistance.

5. Surge suppression varactor shunt on the rectifier diode – this scheme is quite effective, but costly.

6. Dynamic clipper shunt on the rectifier diode – the clipper consists of an R, a C and a diode.



7. Zener shunt on the rectifier diode – may also include a series resistance.



8. Shunt varistor (e.g., GE MOVs) on the secondary – see Figure A1.10.

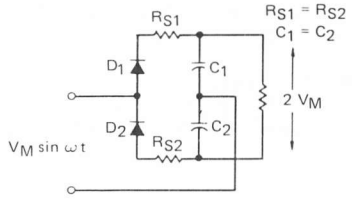
Of the several protective circuits:

- (1), (2), (3) and (4) are least costly, but are limited in their utility to incomplete protection.
- (4) is probably the circuit providing the most protection for the money and is all that may be required in low-current regulated supplies.
- (5), (6), (7) and (8) are most costly, but provide greatest protection. Their use is most worthwhile on high current supplies where high PIV ratings on high-current diodes is costly, or where very high transient voltages are encountered.

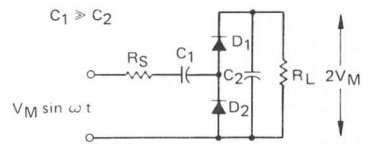
A1.10 Voltage Doublers

Occasionally, a voltage doubler is required to increase the voltage output from an existing transformer. Although the doubler circuits will provide increased output voltage, this is accomplished at the expense of an increased component count. Specifically, two filter capacitors are required. There are two basic types of doubler circuits as indicated in Figure A1.11. Figure A1.11a is the conventional full-wave doubler circuit wherein two capacitors connected in series are charged on alternate half cycles of the line waveform.

Figure A1.11b is a half-wave doubler circuit wherein C_2 is partially charged on one half cycle and then on the second half cycle the input voltage is added to provide a doubling effect. C_1 is normally considerably larger than C_2. The advantage of the half-wave circuit is that there is a common input and output terminal; disadvantages are high ripple, low I_O capability, and low V_{OUT}.



(a) Conventional Full-Wave Voltage Doubling Circuit



(b) Cascade (Half-Wave) Voltage Doubling Circuit

FIGURE A1.11 Voltage Doubler Circuits

These rectifying circuits, being capacitively loaded, exhibit high peak currents when energy is transferred to the capacitors. Filter design for the doubler circuits is similar to that of the conventional capacitor filter circuits. Figures A1.12, A1.13 and A1.14 provide the necessary design aids for full-wave voltage doubler circuits. They are used in the same way as Figures A1.5, A1.6 and A1.7.

A1.11 Design Example

Design a 5V, 3A regulated supply using an LM123K. Determine the filter values and transformer and diode specifications. Ripple should be less than $7mV_{RMS}$. Assume 60dB ripple reduction from typical curves.

1. Establish operating conditions:

   $\omega = 377$ rad/sec

   $V_{IN(PK)} = 18V$ and 10% high line voltage; this allows some 2V headroom before reaching the 20V absolute maximum V_{IN} rating of the LM123K

   $V_{IN(MIN)} = 7.5V$ at 10% low line voltage including effects of ripple voltage

   $V_{IN(DC)} = 11V$ at nominal line voltage; chosen to exceed $V_{IN(MIN)}$ + peak ripple voltage

   $V_{ripple(out)} \leqslant 7mV_{RMS}$

   $V_{ripple(in)} \leqslant 7V_{RMS}$

   $r_{f(in)} \leqslant 7V/11V = 63.5\%$

   $I_{IN} = 3A$

   $I_{IN(MIN)} = I_Q = 20mA$

   $R_L = 11V/3A = 3.67\Omega$

   $R_{L(MIN)} = 7.5V/3A = 2.5\Omega$

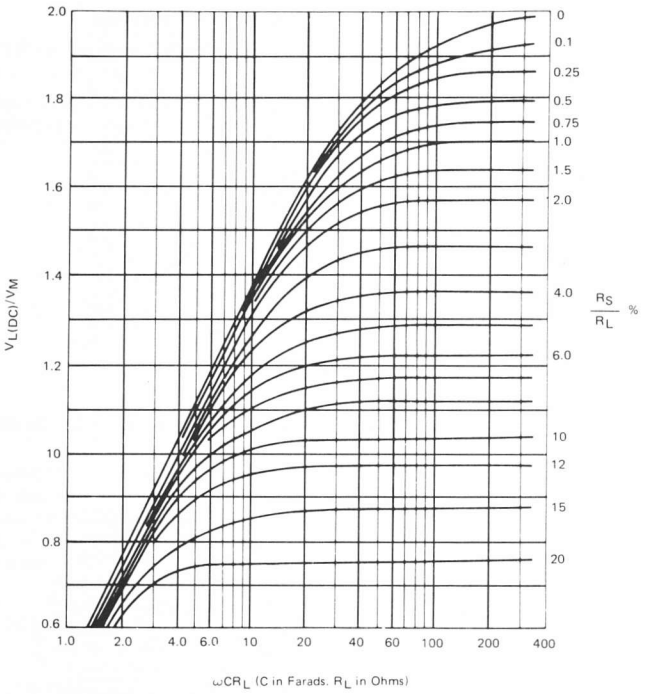


FIGURE A1.12 Output Voltage as a Function of Filter Constants for Full-Wave Voltage Doubler for Full-Wave Voltage Doubler

2. Set:

   V_M = 16.3V nominal, which is 18V – 10% line variation

   $V_{IN(DC)}/V_M$ = 11/16.3 = 0.67

   Assume full-wave bridge rectification because of the high current load. Enter the graph of Figure A1.5 at $V_{IN(DC)}/V_M$ = 0.67 to intercept the "First Approximation" curve.

3. Drop down to the horizontal axis to find $\omega C R_L$ = 3.33.

   Thus, $R_S/R_L \approx 13\%$, or $R_S = 0.4\Omega$ is allowable.

   $$C = \frac{3.33}{3.67 \times 377} = 2400\mu F$$

   (4800μF allowing for –50% capacitor tolerance)

4. Ripple factor is 15% from Figure A1.6. Ripple is then

   $V_{ripple(pk)} = \sqrt{2} \times 0.15 \times 11 = 2.33V$ pk.

5. Checking for $V_{IN(MIN)}$:

   V_M = 16.3V or, allowing for 10% low line voltage, 14.8V

   $V_{IN(DC)} = 14.8 \times 0.67 = 9.91V$

   Subtracting peak ripple, $V_{IN(MIN)} = 9.91 - 2.33 = 7.6V$ which is within specifications

   In fact, all requirements have been met.

6. Diode specifications are:

   $$I_{F(AVG)} = \frac{I_{IN(DC)}}{2} = 1.5A \text{ for FW rectifiers}$$

   I_{FM} = 8 x 1.5A = 12A, from figure A1.7, allowing C = 100% high, for commercial tolerances

   I_{SURGE} = 18V/0.48Ω = 37.5A, worst case with 10% high line, neglecting capacitor ESR

   $I_{F(RMS)}$ = 2.1 x 1.5A = 3.15A, from Figure A1.7, allowing for 100% high tolerance on C

7. Transformer specifications are:

   $$V_{SEC(RMS)} = \frac{16.3 + 1.4}{\sqrt{2}} = 12.6 \text{ for FWB}$$

   (24 VCT for FWCT)

   R_S = 0.48Ω including reflected primary resistance, but subtract 2 x diode resistance

   $I_{AVG} = I_{IN(DC)} = 3A$

   $$I_{SEC(RMS)} = \frac{I_{IN(DC)} \times F}{\sqrt{2}} = \frac{3A \times 2.1}{1.414} = 4.45A$$

   VA rating = 4.45A x 12.6 = 56VA, or 62VA, allowing for 10% high line.

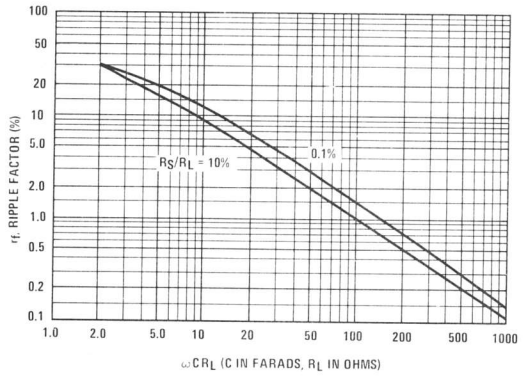
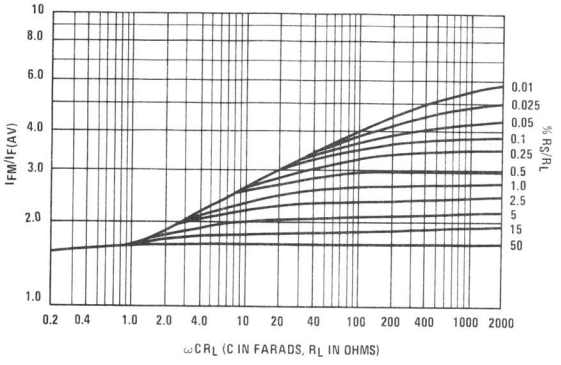


FIGURE A1.13 Ripple as a Function of Filter Constants for Full-Wave Voltage Doubler



RMS Rectifier Current as a Function of Filter Constants for Full-Wave Voltage Doubler

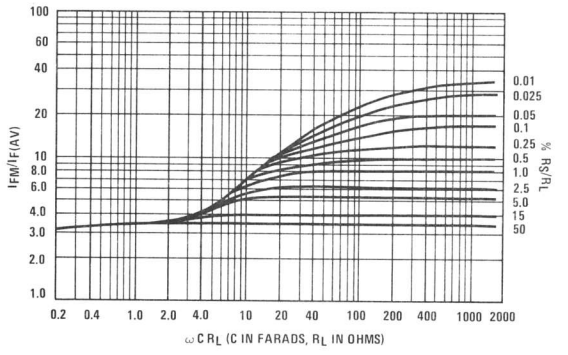


FIGURE A1.14 Relation of RMS to Peak and Average Diode Currents