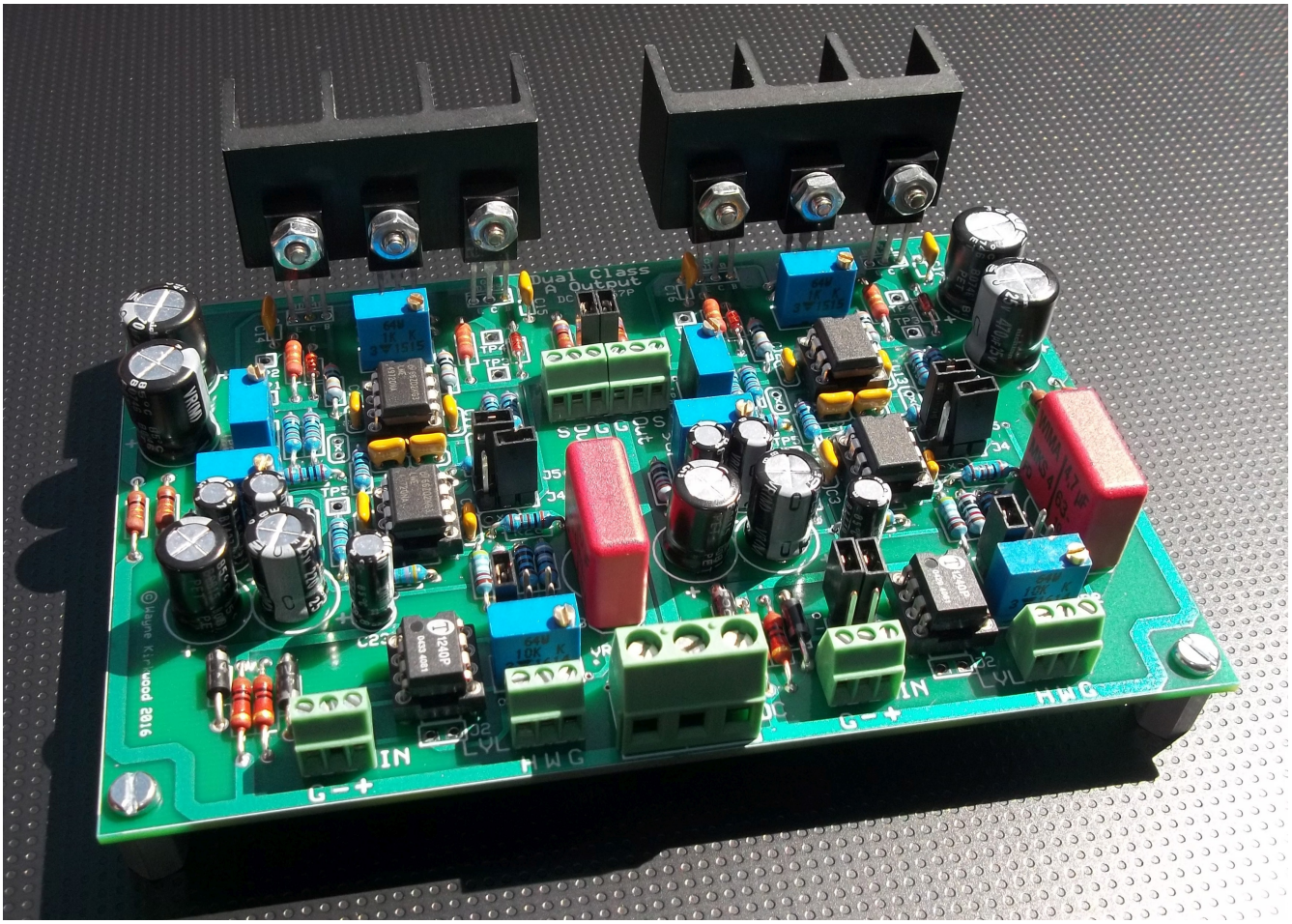
Assembly Instructions for the KA Electronics Dual Class-A II Headphone and Line Amplifier



Dual Class-A PC Board

Install IC sockets

Place the PC Board on the work bench silkscreen side face up.

Drop six 8 pin IC sockets into their respective locations. Observe orientation of the notch. Make sure that you do not place the sockets in the bypass capacitor holes near IC3 and IC6.

Lift the board up and place a piece of cardboard on top of the board to form a sandwich of PC board, sockets and cardboard.

The cardboard is used to hold the sockets in place so the board can be turned over without the sockets dropping out.

Flip the board over.

Tack Solder only two of the corner IC pins. Put downward pressure on the PC board to make certain the sockets are seated on the board as you solder.

Once all the IC sockets are tack soldered, flip the board over.

Make certain that each socket is correctly oriented, fully seated on the

board and square.

If you're satisfied with the placement of the sockets, solder all of the remaining pins. Do not overfill the connection with solder because it can run underneath the socket and form a short between pins.

Visually check each pin's connection particularly those to the ground plane. Reheat any pins if needed. Do not trim the IC socket leads.

Install resistors and diodes

The first fourteen resistors to be installed are "fusible" metal oxide 1W resistors in a 1/4W size. These locations are marked with a **Δ** symbol. Do not use conventional 1/4W film resistors in these locations.

Install four 10R 1W fusible resistors at R1, R2, R3 and R4.

Install four 1R 1W fusible resistors at R5, R6, R7 and R8.

R9 is not used.

Install four 3R3 1W fusible resistors at R10, R11, R14 and R15.

Install two 47R 1W fusible resistors at R12 and R13. *(Note, the 47R value is used in line amplifier builds and as an optional build-out for headphone applications. If you desire a different value of headphone build-out, or are unsure, leave out the 47R resistors at this time. Jumper J6 bypasses these resistors and they may be added at a later time.)*

The following resistors are conventional 1/4W 1% metal film resistors with leads bent on a 0.35" spacing.

Install four 10K 1% resistors at R16, R17, R18 and R19.

Install two 1K 1% resistors at R20 and R27.

Install two 4K75 1% resistors at R21 and R28.

Install two 49K9 1% resistors at R22 and R29. *(Use 49K9 for film coupling caps and FET or bias-compensated op amps such as the LME49720, OPA2134 or OPA2604. For un-bias-compensated op amps such as a 5532 or 2114 use 10K and an electrolytic coupling cap.)*

Install two 20K 1% resistors at R23 and R30.

Install two 100R 1% resistors at R24 and R31.

Install two 909R 1% resistors at R25 and R32.

Install two 3K01 1% resistors at R26 and R33.

R34 and R35 are not used.

Install sixteen 2K 1% resistors at R36 to R51.

R52 and R53 are not used.

Install four 33R 1% resistors at R54, R55, R56 and R57.

Install four 475R 1% resistors at R58, R59, R60 and R61.

Install diodes in the following locations.

Install four 1N4004 diodes at D1, D2, D3 and D4. Observe polarity.

Install four 1N4148 diodes at D5, D6, D7 and D8. Observe polarity.

Install ceramic capacitors

Install ten 100 nF (0.1uF) at C1, C3, C5, C6, C7, C8, C14, C15, C16 and C17.

Install two 10 pF at C2 and C4.

C9 is not used.

Install four 22 pF at C10, C11, C12 and C13.

Do not install capacitors at locations marked with an "X." These are located near IC2, IC3, IC5 and IC6.

C18 and C19 are not used.

Install jumper headers

Install the jumper shunts onto the header pins before you solder them. (The shunts serve as insulators that allow you to position them while soldering without burning your fingers.)

You will need 10 shunts. The shunts are positioned during installation in the locations that will be used in final test.

The shunts should be installed with small openings on the bottom. Some shunts also have openings on the sides. When installing shunts with openings on the sides at J1 and J6, make sure the openings do not face each other or they may short to each other.

With the exception of J1, located only on the right channel, both channels use the same jumper designations for J2-J6.

When installing the headers, tack solder only one pin and reheat it to adjust the position of the header so that its square and flush with the board. Once you're satisfied with the orientation of the headers solder the remaining pins.

Install two four pin (square) headers at J1 and J6. Install two shunts on each header for a total of four. The J1 Shunts should be installed horizontally. The J6 shunts should be installed vertically.

J2 is not normally installed. If IC1 and IC4 are not used, J2 may be linked with a wire and soldered.

Install two 6 pin headers at J3 on both channels. J3 needs shunts installed vertically only on the left row of pins.

Install four 3 pin headers with shunts at J4 and J5. Place the J4 and J5 shunts horizontally on the left-hand pair of pins.

Install Phoenix connectors

When installing the Phoenix connectors make sure the openings for the wires point outward to the bottom edge of the board. When installing the connectors, tack solder only one pin and reheat it to adjust the position of the connector so that its square and flush with the board. Once you're satisfied with the orientation of the connector, solder the remaining pins.

Install four small 3 pin Phoenix connectors at the "IN," and "LVL" locations.

Install a single small 6 pin Phoenix connector at the Output connector. The six pin connector openings should point to the DC power connector away from the jumper links.

Install one large three pin Phoenix connector at the DC location.

Install electrolytic bypass capacitors

Note: The + (positive) terminals for the electrolytic capacitors have a square pad. Where space permits there is also a "+" silkscreen marking.

Install four 220uF 25V polarized electrolytic capacitors at C20, C21, C25 and C26. The polarity of these capacitors are critical.

Install six 47uF 35V polarized electrolytic capacitor at C23, C27, C34, C35, C36 and C37. The polarity of these capacitors are critical.

Install four 470uF 25V polarized electrolytic capacitor at C30, C31, C32, and C33. The polarity of these capacitors are critical.

Capacitors C24 and C28 will be installed in a later step.

Install trim pots

When installing the trim pots be sure to pay attention to the instructions about position of the adjustment screw.

The trim pots should be adjusted to about half their value before installing them to speed PC board testing. Use an Ohmmeter and measure the resistance from one end terminal to the center pin. Adjust the trim pots to approximately half the label value.

When installing trim pots, tack solder only the middle pin and be certain the body of the trimmer is aligned properly before soldering the remaining pins.

VR1 and VR2 are optional and are used to provide a trimmed input level. If the DCAO2 is going to be used with an external level control or fixed level input, VR1 and VR2 may be omitted.

If VR1 and VR2 are desired, install two 10K trim pots at those locations. The trims should be installed with the adjustment screw on the right.

Install two 50K Ohm trim pots at VR3 and VR4. The screw adjustment should be on the right.

Install two 200 Ohm trim pots at VR5 and VR6. The adjustment screw should be at the top.

Install two 1K Ohm trim pots at VR7 and VR8. The adjustment screw should be on the right.

Install the coupling capacitors

C24 and C28 are the input coupling capacitors and may be 5 mm bipolar electrolytic, 10 mm box film or 15 mm box film.

A coupling capacitor is recommended to prevent DC offsets in the input line receiver from appearing in the output and wiper of the level control. The DCAO2 may be direct coupled in which case C24 and C28 are wire links.

The choice of film or electrolytic coupling depends on the type of op amp used for IC2 and IC5. Bias current compensated and FET input op amps are better suited for using film capacitors because they permit higher values of R22 and R29.The bill-of-materials specifies bias-compensated LME49720 op amps for IC2 and IC5. R22 and R29 are 49K9 and C24 and C28 are 4.7 uF 15 mm. These same values are suitable for FET input op amps such as the OPA2134, OPA2604 and a bipolar OPA1612 or FET OPA1642 on a surface mount to DIP adapter.

If an NE5532, NJM2114 or other high bias current op amp is used, R22 and R29 should be 10K and coupling capacitor values of 47 uF (bi-polarized) used for C24 and C28.

Install two 4.7uF 63V film capacitors (or electrolytic as noted above) at C24 and C28.

Note: Do not install the ICs at this time.

Check all solder connections and reheat or re-flow them if necessary

When component leads are trimmed after soldering the solder joint becomes fractured. It is always a good idea to reflow all solder connections while checking for bridges or pins which may have missed being soldered.

If you add solder during this step do so sparingly particularly under IC sockets. Solder can flow through the PC board vias to the underside of the IC socket and cause shorts between pins.

If you prefer to remove the solder flux residue from the PC board now is a very good time to do it.

When you're finished inspect every joint under magnification.

Initial Tests

The board should be tested on a power supply before installing the ICs and output transistors.

Initial DC Tests

Connect a source of bipolar DC power.

If a variable power supply is used, slowly raise the voltage to about +/-15V.

There should be no measurable current draw. If excess current is drawn check the board for solder bridges and correct polarity of D1, D2, D3, D4 and all the electrolytic capacitors.

Check the voltages at pin 7 of IC1 and IC4. It should be +15V. The voltages at pin 4 should be -15V.

Check the voltage at pin 8 of IC2, IC3, IC5 and IC6. It should be +15V. The voltages at pin 4 should be -15V.

The following steps check the voltages at the output transistor PC board terminals before they are installed.

Check the voltages at the collectors of Q1 and Q4. It should be -15V.

Check the voltages at the collectors of Q3 and Q6. It should be +15V.

Check the voltages at the bases of Q1, Q3, Q4 and Q6. They should read 0V.

Check the DC voltages at the collectors of Q2 and Q5. It should be about +3.5V but will vary with the setting of VR7, VR8 and the supply voltage.

Check the DC voltages at the bases of Q2 and Q5. It should be about 2.4V and will also vary with the setting of VR7, VR8 and the supply voltage.

If any of the voltages are out of range look for solder bridges or an unsoldered pin or component lead.

Remove power.

Install the ICS

Install two THAT1240 (or THAT1246 ICs at IC1 and IC4.

Install four LME49720 ICs at IC2, IC3, IC5 and IC6.

Offset and Current Draw Tests

Reconnect power.

If a variable power supply is used slowly raise the voltage to about +/-15V.

Measure the DC voltages of the IC pins listed below. No input or output should be pinned to a supply rail.

The DC offset at pin 6 of IC1 and IC4 should be less than 10 mV.

The DC voltage at pin 1 of IC2 and IC5 should be about 3.5V.

Note: J4 should be in the left-hand position for the following test.

The DC offset of pin 7 of IC2 and IC5 varies depending on the adjustment of VR3 and VR4. Adjust VR3 and VR4 to obtain a value as close to 0V as you can at pin 7 of IC2 and IC5. The open top of the jumper shunt is connected to pin 7 and may be used to measure these voltages.

Measure the DC voltages at pin 1 of IC3 and IC6. They should be approximately -3.5V.

Measure the DC voltages at pin 7 of IC3 and IC6. They should be approximately +3.5V.

The driver supply current is typically 30 mA per channel. Measure the voltage drop across R1 and R3, the 10 Ohm resistors. It should measure less than 300 mV. (10mV per mA).

Disconnect DC power.

Install the output transistors

The DCAO2 bill-of-materials does not contain a heat sink and it is necessary to make one or obtain two CTS 7-342-1PP or CTS 7-342-2PP. The "-1PP" is shorter and about 10 degrees C per Watt; the "-2PP" about 5 degrees C per Watt. If the CTS or an equivalent is not available one, can be made out of aluminum or copper bar stock usually available at most home supply stores.

Q1-Q3 and Q4-Q6 must be thermally-coupled and adequately heat sinked. If it is more convenient to construct it is not necessary for the left and right sets of transistors to be on two separate heat sinks.

Pre-fabricate the heat sink assembly in order to use it as a jig before soldering Q1-Q6 to the PC board. The heat sink allows the devices to be held while they are positioned and soldered. Q1-Q3 and Q4-Q6 are spaced on 0.50" centers. The space between the center line of Q3 and Q4 is 1.30".

If the heat sink has fins they should be pointing away from the board when installed.

The part number on the transistors should be facing up. Heat sink grease and insulators are not required if using the insulated Fairchild BD139 and BD140 transistors specified in the bill-of-materials. Other BD139/BD140 transistors may not be insulated and may require mounting kits.

Mount, in order of left to right, two sets of three transistors on the flat side of two heat sinks. The order is: Q1 BD140, Q2 BD139, Q3 BD139, Q4 BD140, Q5 BD139 and Q6 BD139 using 4-40 x 1/2" screws, fiber washers and nuts.

Loosely tighten the screws so the transistors are snug but can be adjusted to align them to the board.

Double-check the order of the transistors: BD140 > BD139 > BD139 and BD140 > BD139 > BD139.

Feed the transistor/heat sink assembly leads into the PCB board and adjust the transistor alignment before tack-soldering one transistor pin.

Solder each transistor's middle lead and adjust the alignment of each device before soldering the remaining leads.

Install four 3/8" hex spacers using four 4-40 x 1/4" screws and fiber washers. Set the remaining four screws and fiber washers aside for installation of the board into a chassis.

DC Tests with the output transistors installed

Reconnect power.

If a variable power supply is used slowly raise the voltage to about +/-15V.

Check the power supply to make sure the total current being drawn by both channels is less than 300 mA.

Measure the DC voltage at TP5 on both channels. It should read approximately 800-850 mV.

Measure the DC voltage at the outputs. It should read less than 50 mV.

The DC offset will be adjusted in a later step.

Set the idle current

The recommended idle current for headphone applications is 90-100 mA per channel. Line amplifier applications with high impedance loads can use lower current.

The following instructions set the final idle current to approximately 90 mA. The idle current may be calculated by V/3.3Ω where V is the voltage measured between TP1 and TP2 (BD140 PNP) or TP3 and TP4 (BD139 NPN). The idle current prior to warmup is adjusted to a slightly higher value of 100 mA.

Measure the voltage from TP1 (meter ground) to TP2 (meter plus). It should read approximately -200 mV. Adjust VR7 for -330 mV across TP1 and TP2. Measure the voltage from TP3 (ground) to TP4 (meter plus). The voltage from TP3 to TP4 should be roughly equal to TP1/TP2 and about +330 mV.

Repeat the previous procedure for the right channel by adjusting VR8.

The heat sinks will become warm to the touch. The idle current has a negative temperature coefficient and should be checked and re-adjusted if necessary after a 15 minute warm-up. Measure the voltage from TP1 (meter ground) to TP2 (meter plus). After warmup the voltage should be about -295 mV corresponding to an idle current of about 90 mA. The voltage from TP3 to TP4 should be roughly equal to TP1/TP2.

A small amount of drift with ambient temperature is normal.

Measure the DC voltage at TP5. It should be approximately +920 mV.

Move J4 to the right-hand jumper position.

Measure the DC voltage from the output terminals to ground. Adjust VR3 (left) and VR4 (right) to have an offset less than less than 1 mV. The offset should be adjustable to less than 100 uV.

A quick check of the output idle current can be made at the 1Ω resistors designated R5 and R8. A 90 mA current will read 90 mV. (1 mV per mA.)

The output idle current and offset do not interact but both should be re-checked after warm-up.

This completes initial DC tests and idle current adjustment.

Signal Tests

This section performs signal tests to verify basic functionality, operation of the jumpers and to adjust the calibration of VR1 and VR2 input trims and VR5 and VR6 AC balance adjustments.

The jumpers at J1 should be installed horizontally, with "-" to "-" and "+" to "+" to drive the right channel from the left input.

J3 should be in the left-most vertical position.

J4 should be in the right-hand position.
J5 should be in the left-hand position.
J6 should be installed vertically in both positions.

Connect a short jumper from the Left In Phoenix connector from "-" to G.

Apply +/-15V power and confirm the bias current and offset adjustments performed previously.

The following tests require an AC voltmeter and a signal generator. If you have an oscilloscope you may also connect it to the outputs to monitor the following tests.

Connect a signal generator to the Left In "+" and "G" terminals. Apply a 1 kHz signal at -8 dBu. (Approximately 309 mV). (For THAT1246 line receivers use -2dBu.)

Measure the output level from the Out connector to ground. The level should be be +4 dBu (775 mV).

Move J3 to the middle position to enable the input level trim VR1 and VR2. Adjust VR1 and VR2 until the output level reads -2 dBu on each channel. The final adjustment of VR1 and VR2 will be done on installation; this test verifies operation, sets the initial attenuation to -6 dB and balances the levels between channels.

Move J3 to the right-most position. There should be no output on either channel.

Temporarily connect a link from the Level Phoenix connector (LVL) from the "H" (hot) to the "W" (wiper) terminals. Output should be observed when the link is installed. (Use a wire inside the connector because the screw terminals on the top of the Phoenix connector do not provide reliable connections unless they are tightened.)

Move J3 back to the left-most position.

Move J5 to the right-hand position. Measure the output level. It should read -8 dBu.

Move J5 back to the left-hand position.

Move J4 to the left-hand position.

Measure the Output level. It should measure +4 dBu.

The following step adjusts the AC balance so that the electrical gain of the pre-driver is balanced between the upper NPN and lower PNP halves. To easily measure the balance, a differential ungrounded measurement is made between test points TP2 and TP4. When there is close electrical balance a null is formed. When out-of-balance a voltage appears between them.

To perform the AC balance test, a floating (ungrounded) AC-coupled AC voltmeter is required. A common battery-powered DVM if it has response to 1 kHz is ideal for this test. Make certain that the voltmeter does not respond to DC when measuring AC. If it does, a coupling capacitor will be required in series with one meter lead. If the capacitor is polarized, make certain that the positive terminal is connected to TP4.

Set the AC voltmeter to the lowest (200 mV) scale. Connect a floating AC voltmeter (DVM) to TP2 and TP4. Allow a few seconds for the DC to bleed off the meter's internal coupling cap and the meter to settle.

Adjust VR3 for the minimum AC voltage. There will be a null point as VR3 is rotated from one extreme to the other. Adjust for the minimum voltage that the meter will resolve. It should easily be adjustable to less than 1 mV.

Repeat the process for the right channel and adjust VR4.

Move J4 on both channels back to the right-hand position.

The following sequence of tests check the operation of J1.

Measure the AC voltage using a floating meter between the Left and Right Channel outputs. It should be very low. (The error is small and due to gain mis-match.) If you would like to precisely balance channel gains, adjust the right channel slightly to match the left by nulling the reading to as close to 0 volts as possible.

Switch the orientation of J1's shunts from horizontal to vertical. This configures the two outputs in bridged, "out-of-polarity," configuration.

Measure the AC voltage between the Left and Right channel outputs. It should measure about +10 dBu. (2.45V.)

Remove the shunts from J1 and re-install them only on one pin (to prevent loss) in a "stored" position. When installing shunts on J1 and J6 make certain that the open portion of the shunt (on the side) does not touch the open side on the adjacent shunt.

This completes basic signal tests.

Output load tests

Install J1 with the jumpers horizontally.

Connect 33 Ohm 1W resistors from the Out to G terminal on the Left and Right Channels.

Feed a low distortion source of 1 kHz at -6 dBu into the left channel input. (0 dB if using THAT1246 inputs.) This should produce +6 dBu at both outputs. (1.55 V rms).

Jumper Descriptions

J1 Input strapping for the right channel.

Note that when using J1 make certain that any openings on the shunts point outward. Otherwise, the + and - inputs may short together.

If J1 is jumpered horizontally "+" to "+" and "-" to "-" the right input is fed from the left input connector and the outputs are in polarity. Used for test, to feed two mono outputs such as a distribution amplifier, or to parallel two outputs for higher current in conjunction with J6.

If J1 is jumpered vertically "+" to "-" on both locations the right input is fed from the left input connector and the outputs are out-of-polarity. Used for

balanced differential outputs and “bridge-tied-load” BTL connection.

J2 IC bypass.

J2 bypasses the balanced input ICs when they are not used. J2 is normally not installed. There is a J2 for both channels.

J3 Level Control.

J3 selects the Level control device. There is a J3 for both channels

When J3 is fitted vertically in the left-most A position the balanced input is directly connected to the gain stage. Level control, if any, is provided ahead of the DCAO2.

When J3 is fitted vertically in the middle B position, the on-board level trims, VR1 and VR2, adjust the output level. The on-board level trim is ideal for transformer drivers to compensate for insertion loss or in distribution amplifier applications to adjust output level.

J3 fitted in the right-hand most C vertical position transfers gain control to the Level (LVL) Phoenix connector for use with external volume controls. The terminals are marked “H” for the hot end, “W” for the wiper and “G” for signal common. The minimum value for an external potentiometer should be 5KΩ with VR1 and VR2 fitted and 2KΩ if VR2 And VR2 are not fitted.

J4 Feedback Mode.

J4 determines whether the final output stage runs open or closed loop. At power levels below 100-200 mW the output stage may be run open loop, in Class-A, with very low distortion. Closed loop operation permits very low distortion, in Class A/B, at power levels in excess of a Watt.

Closed loop operation at low power levels doesn't reduce distortion significantly, but does provide the advantage of greatly reduced output impedance in headphone amplifiers. The open loop output impedance of the DCAO2 is about 2Ω throughout the audio band. When the DCAO2 is operating closed loop, the output impedance is about 50 times lower from DC to mid-band at 40 mΩ rising to only 70 mΩ at 20 kHz.

Build-out resistance is desirable for direct and transformer-coupled line outputs so the reduction in output impedance from global feedback may not benefit performance.

J4 should always be fitted so that IC2 and IC5 operate closed loop.

J4 in the left-hand position receives feedback directly from the gain stage causing the output stage to run open loop.

When J4 is in the right-hand position feedback is taken from the output.

J5 Pre-driver Input.

J5 selects the source signal for the pre-driver stage.

When J5 is in the left-hand A position IC2 and IC5, which provide gain and feedback correction, are in the signal path and feed the pre-driver.

J5 installed in the right-hand B position allow the balanced input to drive the pre-driver directly. Gain and feedback are not available.

J6 may be jumpered three different ways. Note that when using J6 make certain that any openings on the shunts point outward. Otherwise, Left and Right may short together.

When J6 is open at both locations there are 47Ω build-out resistors in the signal path. J6 should be open for driving balanced audio lines. If a different value build-out is desired for driving transformers, R12 and R13 should be changed.

When J6 is linked vertically in both locations the build-out resistors are shunted the output impedance is either 2Ω (open loop) or "0 Ohm" (closed loop.)

If J6 is linked horizontally across the bottom two pins, the two outputs are paralleled and can provide twice the amount of current. R12 and R13 ballast the two outputs to prevent circulating currents and may be reduced in value. When operating the DCAO2 in this configuration the left and right channel gains should be closely matched and the offsets trimmed.

Detailed Parts List

A complete bill of materials is available from Mouser Electronics Project Manager application:

https://www.mouser.com/ProjectManager/ProjectDetail.aspx?AccessID=b5edbf3bcb

Other Resources

Pro Audio Design Forum Build Thread:

http://www.proaudiodesignforum.com/forum/php/viewtopic.php?f=7&t=825

For more information contact: sales@ka-electronics.com

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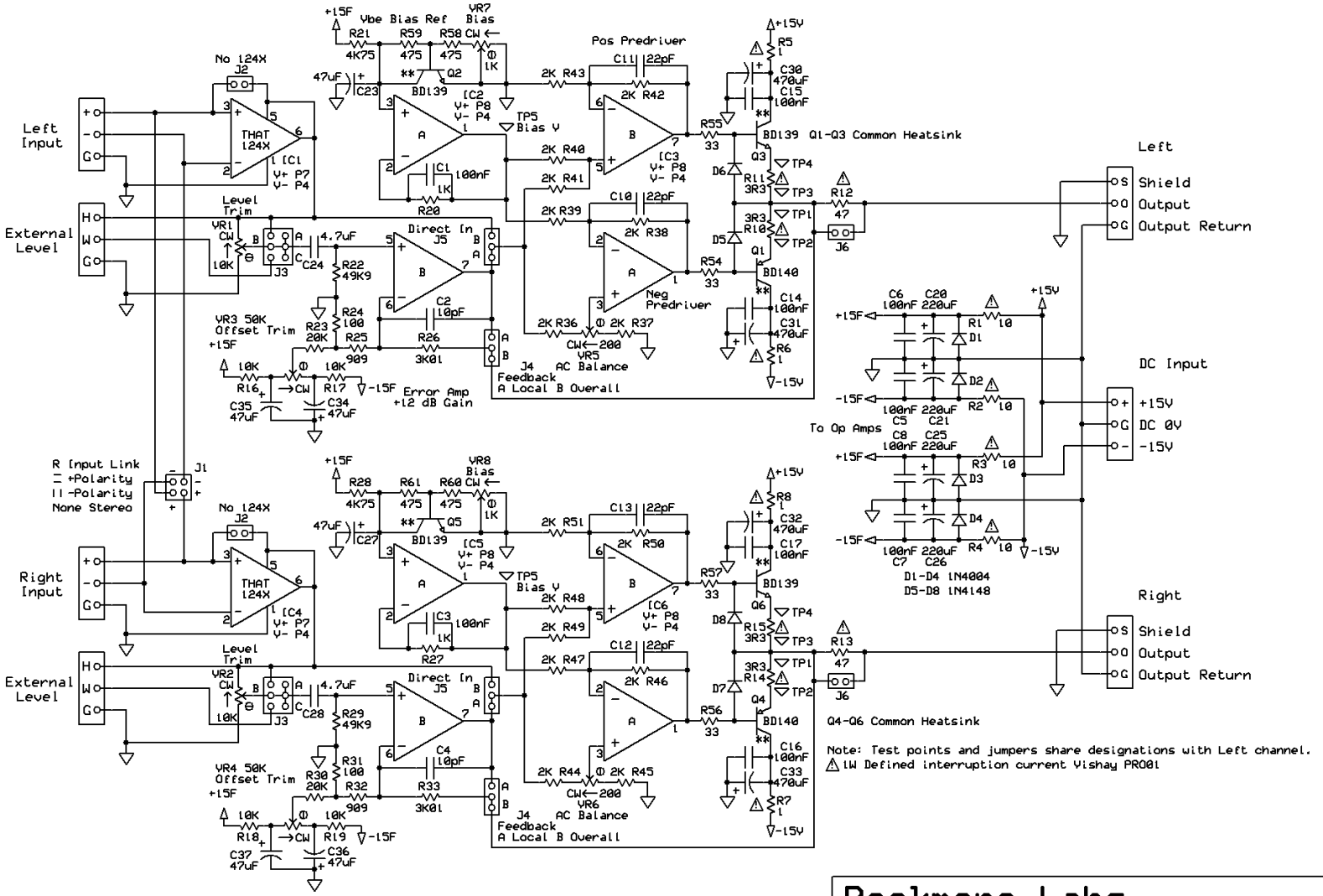
Headphone and Line Amplifier



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Dual Class-A II Line Amp		
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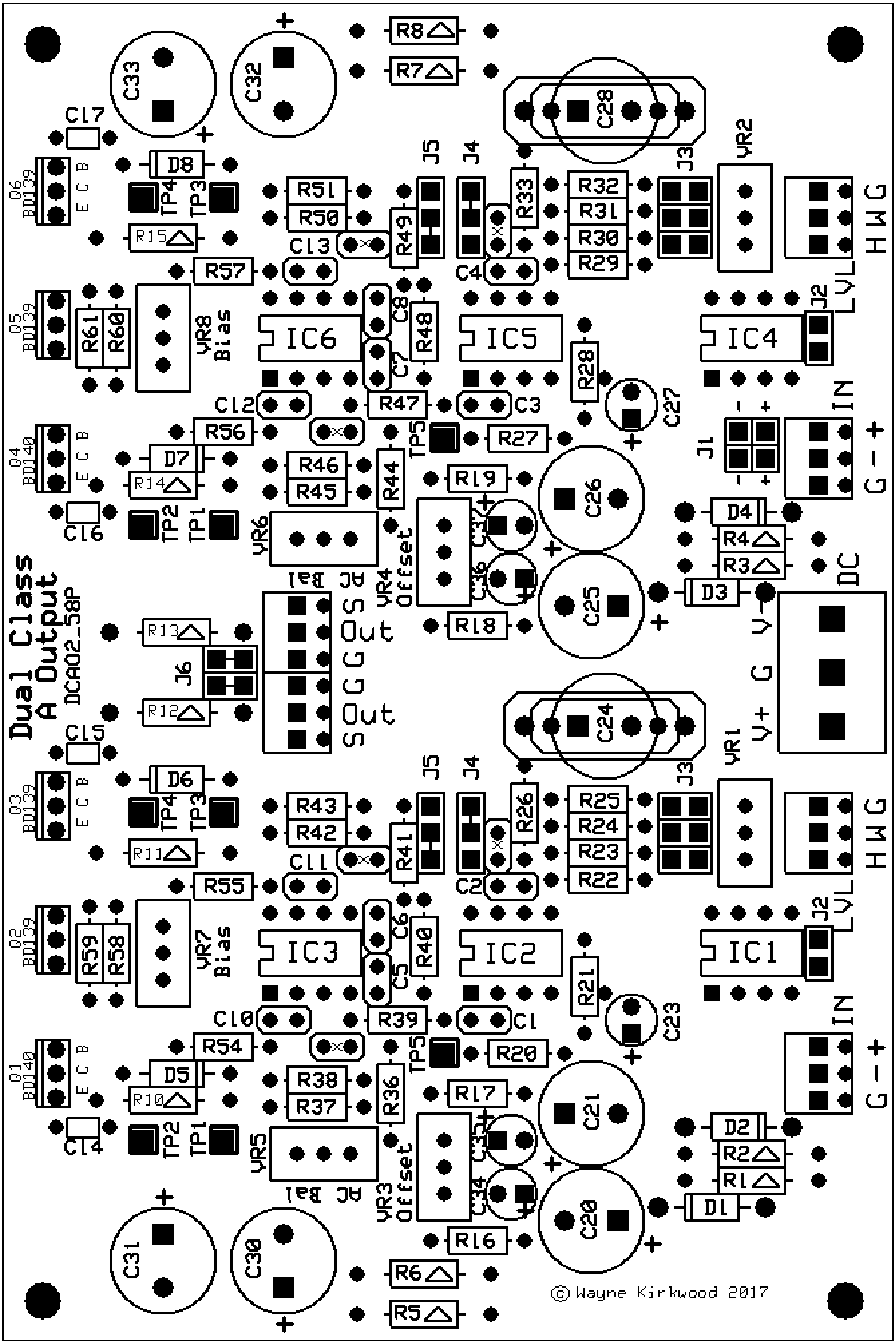
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A Output
DCAO2_58P
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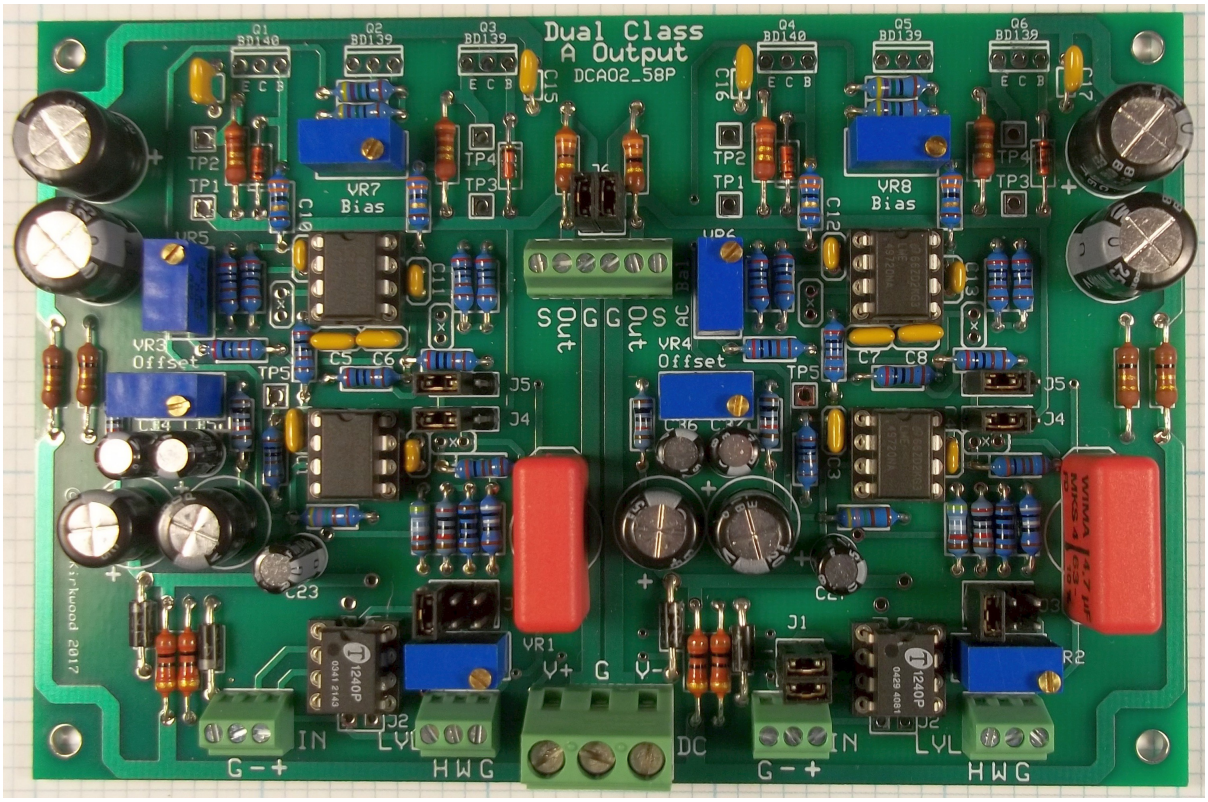
Dual Class
A Output
DCA02_58P
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BD139
Q3
BD139
Q4
BD140
Q5
BD139
Q6
BD139
VR7
Bias
VR8
Bias
VR3
Offset
VR4
Offset
VR5
VR6
VR1
VR2
TP1
TP2
TP3
TP4
TP5
J1
J2
J4
J5
C5
C6
C7
C8
C23
Out
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