Siliconix

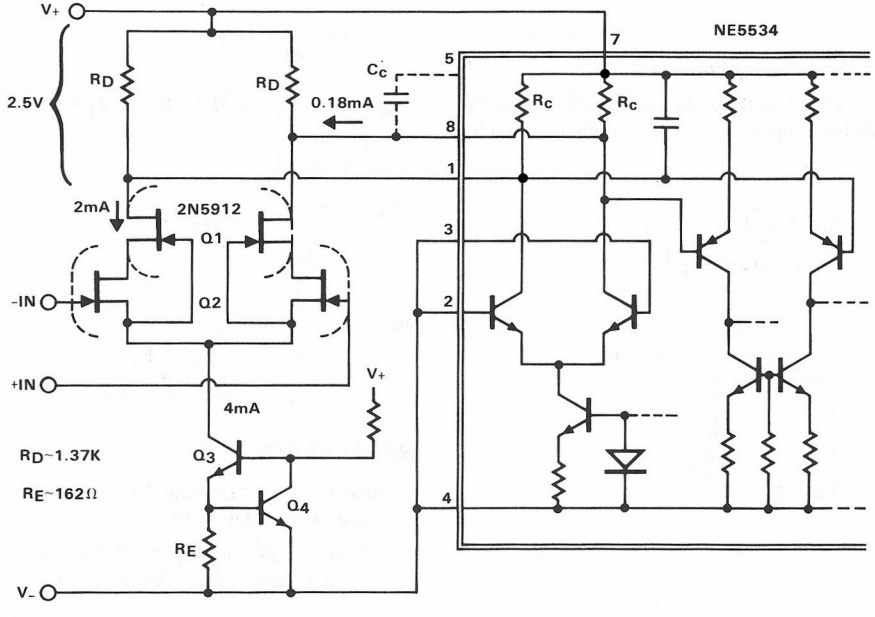
APPLICATION NOTE

Composite Op Amp for High Performance

For op amp applications requiring the best possible performance, consider a composite op amp that takes advantage of differing process technologies. A JFET dual can be combined with a Signetics NE5534 bipolar op amp for outstanding performance. Input bias current can be reduced, yet slew rate can be very high (20V/μsec to 40V/μsec) and the circuit is unity-gain stable. Output swing is a minimum of ±12V into a 600 ohm load when operating from ±15V power supplies. This high output capability combined with a JFET input stage makes this an excellent amplifier for high-speed integrators, SAMPLE/HOLD circuits, peak detectors, and log amplifiers.

The input portion of the circuit is shown in Figure 1. The NPN input stage of the NE5534 IC op amp is biased into cut-off by connecting both inverting and non-inverting inputs to the negative rail. A JFET preamplifier input stage

High Performance Op Amp Using The Siliconix 2N5912



is then connected into the PNP second stage of the NE5534 and the currents that formerly flowed through the NE5534 NPN input pair are now diverted into the JFET input pair. Drain resistors R_D effectively parallel the collector resistors R_C from within the IC op amps and the JFET drain currents will then be the sum of the currents through R_D and R_C. The voltage across the parallel combination of R_D and R_C is nominally 2.5V due to the internal biasing of the NE5534. Going directly into the second stage of the IC op amp rather than into the NE5534 NPN input stage has two distinct advantages:

1. Frequency response is better in that the phase shift of the bipolar input stage is avoided. A high-current JFET input stage, such as the 2N5912 when operated in the 1mA to 8mA drain current range, has excellent frequency response in comparison to an NPN stage operating in the 150μA to 200μA range.

2. The operating level at the JFET drains is only 2.5V below the positive supply rail, therefore the common-mode input range for the JFET input stage can be relatively high. The combination of low input bias current with high frequency response is useful for SAMPLE/HOLD circuits, high-speed integrators, photo-multiplier tube amplifiers, and high-speed data conversion circuits.

Although more expensive than a single monolithic op amp, the combination of a JFET preamp with a bipolar IC second stage can provide substantially better performance than any monolithic alternatives.

A Siliconix 2N5912 JFET dual was chosen for the input stage in this example because of its high operating current range, high gain, and excellent frequency response. The saturation drain current I_{DSS} has a specified range of 7mA to 40mA, but is typically 10mA to 24mA. Gate source cutoff voltage $V_{GS(off)}$ is in the range of -1V to -5V with a typical value of approximately -2V to -4V. The 2N5912 characterization curves indicate that any drain current from 1mA to 8mA will provide good performance, and 2mA was chosen for this application.

The current diverted from the bipolar input stage to the JFET input stage is nominally 180μA on each side; therefore a drain current on each side of 1.82mA is needed from the drain resistors R_D to make up a total drain current of 2.0mA. The drain resistor R_D therefore needs to be approximately 2.5V/1.82mA, or 1370 ohms on each side.

Gain of the JFET input stage can now be calculated. From the 2N5912 characterization curves, forward transconductance g_{fs} will be in the range of 2.6mmhos to 5mmhos for units having I_{DSS} of 10mA to 24mA and when operated at a drain current of 2mA. The differential gain can be approximated by the product $g_{fs} R_D$. Using a center value of 4.3mmhos and 1230 ohms, (R_D and R_C in parallel), then the gain will be approximately 6.5, or 16dB. Total amplifier gain was found to closely approximate the gain curve for a 5534 being operated alone.

The cascode configuration using two input pairs as shown has several advantages. Most importantly, the input gate current is dramatically reduced due to the lower drain-to-gate voltage on the input pair. In the cascode configuration, the gate-to-source voltage on the upper pair will be the drain-to-source voltage of the input pair even with the common-mode input variations. All of the common-mode swing is taken up by variations in V_{DS} of the upper pair. Gate leakage of the input pair is primarily dependent on drain-to-gate voltage V_{DG}, which will be a constant $-2V_{GS}$ in this cascode configuration. Drain-to-gate voltage on the input pair will be low, typically in the 3V to 6V range, which is well below the "I_G breakpoint". From the characterization curves on the 2N5912, gate current leakage will be under 2pA for drain-to-gate voltages under 6V. The cascode configuration is very effective in reducing input bias current for JFET input stages. Another advantage of the cascode configuration is a reduction of input capacitance. The input pair drains are "bootstrapped" to the common source point and both must follow the gate voltage. The effective capacitance from gate-to-drain and from gate-to-source is reduced. In addition, output conductance is reduced by the cascode configuration which also helps CMR. Adding the second JFET pair significantly improves both input bias current and common-mode rejection without degrading other parameters.

The constant current source consisting of Q3 and Q4 primarily improves common-mode rejection and rejection of power supply variation. It also establishes the nominal operating voltage at the input (pins 1 and 8) of the 5534 op amp. The current will be a constant V_{BE}/R_E independent of fluctuations in power supply voltage or input voltage level. This current source has very high impedance, therefore common-mode inputs are heavily attenuated.

Common-mode-rejection-ratio (CMRR) is very high due to the use of a constant current source, but can be further improved by matching of drain resistance. The parallel combination of R_D and R_C is the effective drain resistance for this design. The transconductance ratio between the two sides of the input pair also directly affects CMRR. The drain resistors should be well-matched to minimize the CMRR adjustment range since it also affects offset and drift.

Each 1% mismatch in drain resistance will cause approximately 11μV/°C of input offset voltage drift. CMRR can be readily trimmed to over 100dB. CMRR vs. frequency is excellent due to the use of the 2N5912, a wide-bandwidth FET, in a cascode configuration.

A high performance op amp should also have good output characteristics, low noise, and high slew rate. The NE5534 op amp is rated for ±14V mimimum output swing into a 600 ohm load when operating from ±15V power supplies. Output resistance is typically 0.3 ohms. The Siliconix

2N5912 characterization curves show a typical equivalent input noise voltage of only $10nV/\sqrt{Hz}$ at 10Hz. There is also a component of noise from the second stage, but its effect is divided by the input stage gain and its contribution is small. Input current noise of this composite op amp is very low due to the typical operating level of 1pA input bias current. For slew rate, this circuit is capable of $50V/\mu sec$ when going negative. Positive slew rate is $50V/\mu sec$ without use of a compensation capacitor, but drops to $25V/\mu sec$ with a 20pF compensation capacitor. Compensation capacitance will generally be needed only when driving capacitive loads. Even the lower value of slew rate, $25V/\mu sec$, corresponds to a full-power (±10V) frequency of 400KHz.

While the vast majority of op amp applications can be satisfied through use of conventional IC op amps, there are applications in high-performance instrumentation systems that require superior performance. This composite op amp, which makes use of precision dual JFET input pairs and a high performance IC op amp, provides a unique combination of low input bias current, high CMR, low noise, excellent frequency response, and high output swing.