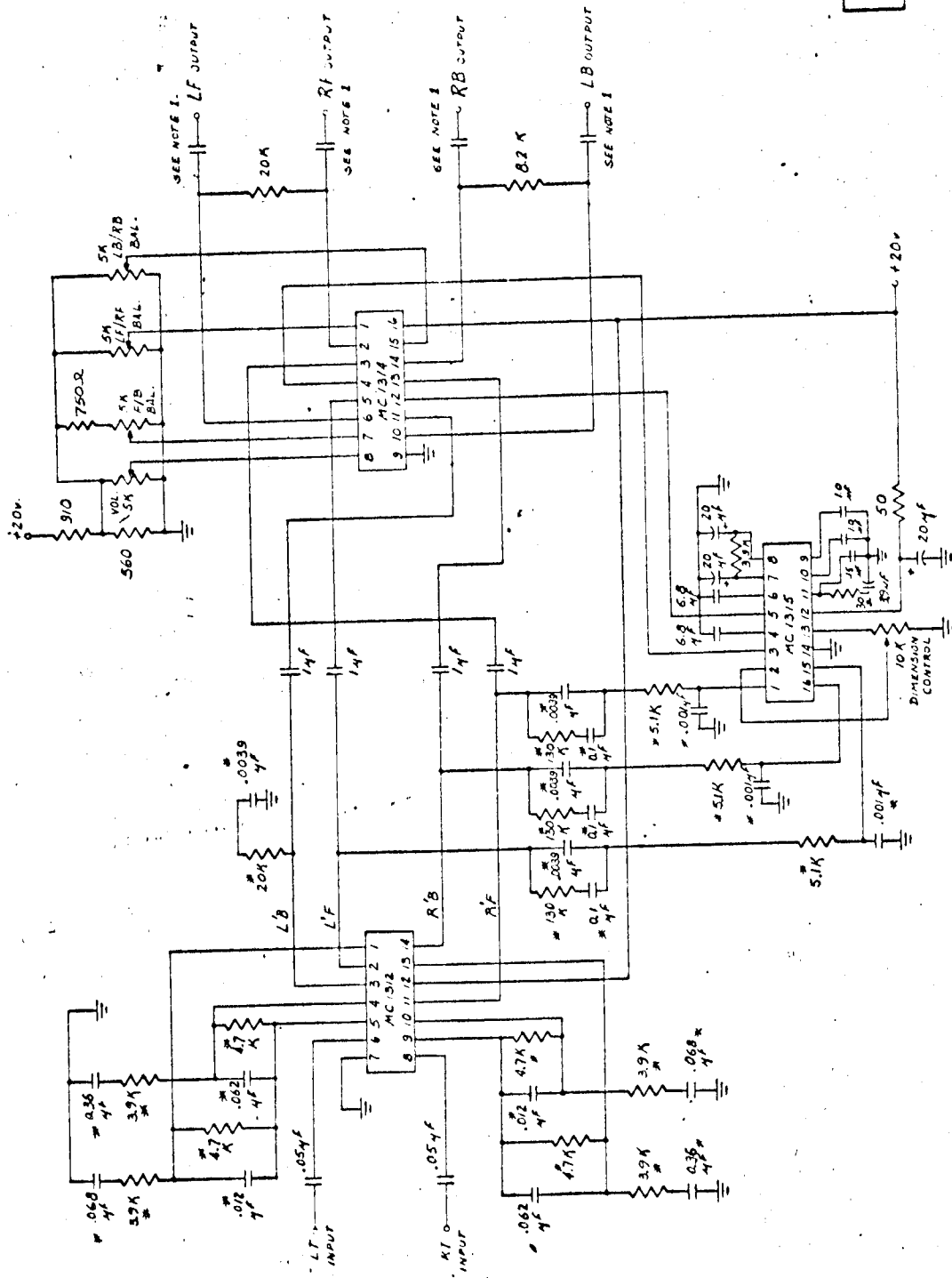


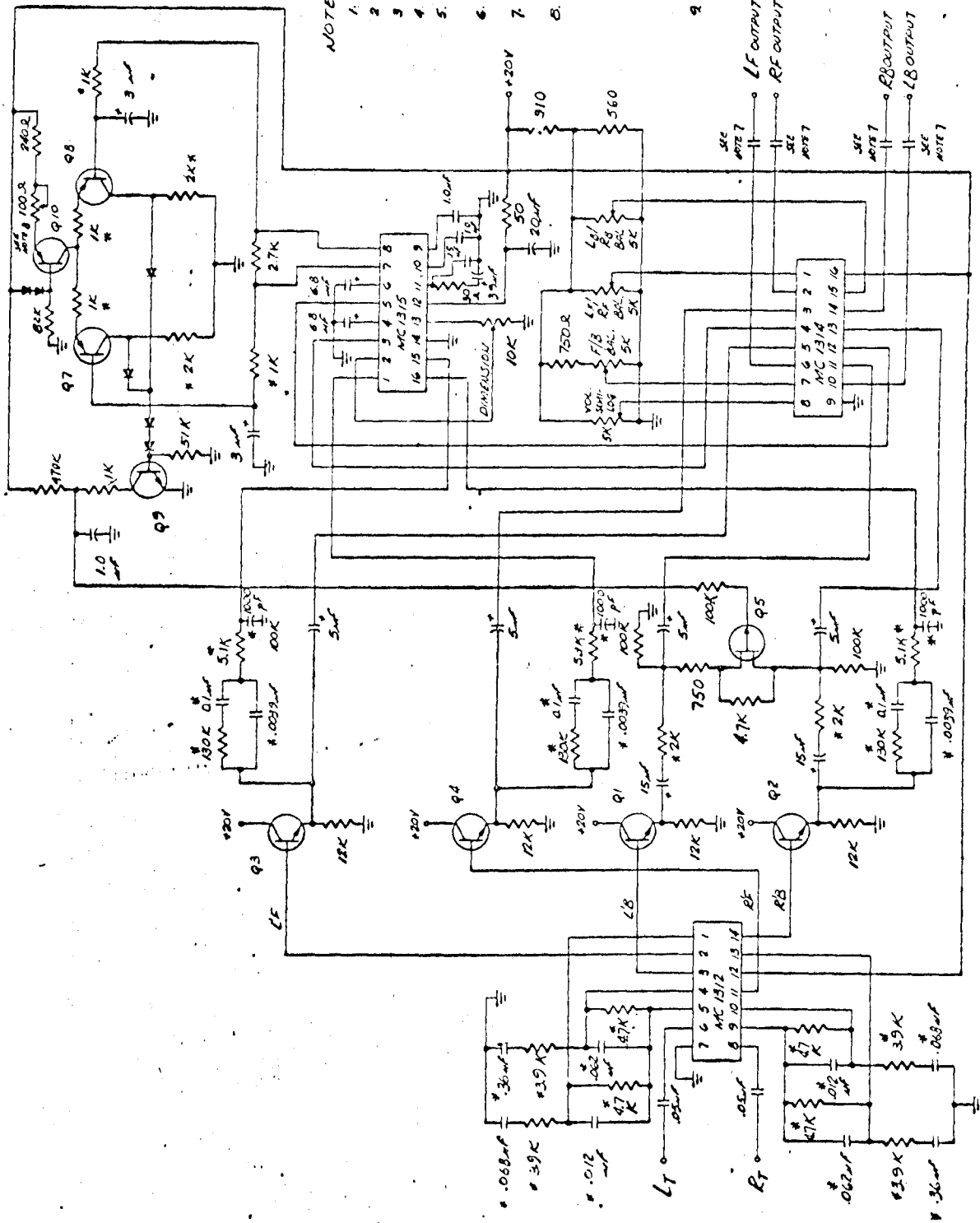
VARIABLE BLEND SQTM FULL-LOGIC DECODER, L-2
USING MOTOROLA INTEGRATED CIRCUITS

March 4, 1974



- NOTES: (UNLESS OTHERWISE SPECIFIED)
1. COUPLING CAPACITOR VALUE DEPENDS ON LOAD OF FOLLOWING &
 2. ALL COMPONENTS MARKED # ARE 5% TOLERANCE.
 3. POWER SUPPLY, +20VDC @ 75 mA

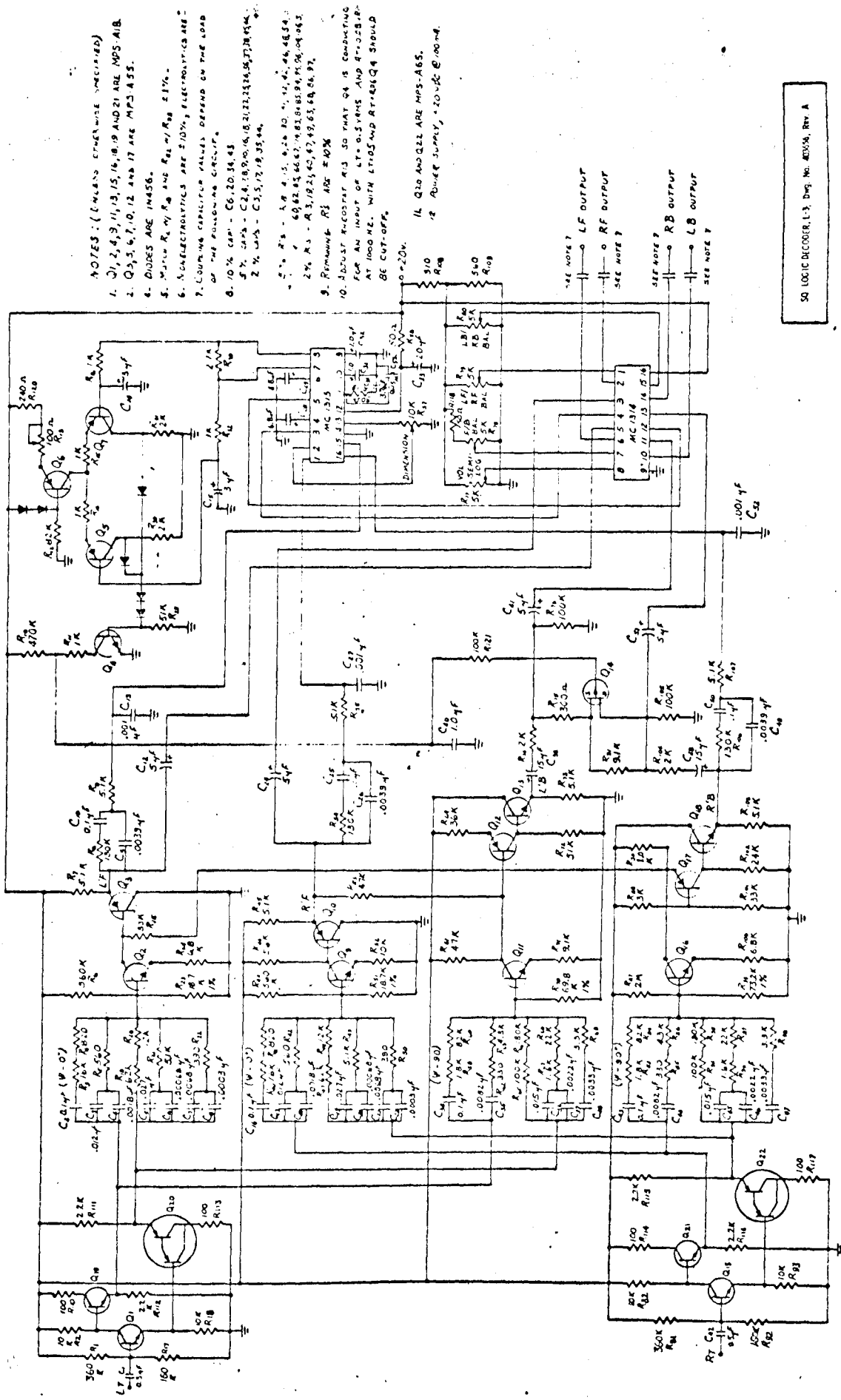
SO LOGIC DECODER, L-1; Dwg. No. 4035A, Rev. B



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. Q1,2,3,4,9 ARE MP5A10
2. Q5,6 ARE 2N5401
3. Q7,8,10 ARE MP5A55
4. ALL DIODES ARE M456
5. RL SEM. CAP; F/B CAP.; L1/R1, RM;
L2/R2 CAP. ARE 5% LINEAR POTS
6. ALL COMPONENTS MARKED * ARE
5% TOLERANCE
7. COUPLING CAPACITOR FOR VALUE DETERMINED
ON LOAD OF FOLLOWING CIRCUIT
8. ADJUST 100Ω RHEOSTAT SO THAT
Q9 IS CONDUCTING FOR AN INPUT
OF LT = 0.5 Vrms AND RT = 0.20 Vrms
AT 1KHz. WITH LT = 0.5 Vrms AND
RT = 0.06, Q9 SHOULD BE
CUT-OFF.

9. POWER SUPPLY; +20VDC @ 75 mA



- NOTES: (VALUES OTHERWISE SPECIFIED)
- Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12 AND Q13 ARE MPS-A18.
 - Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12 AND Q13 ARE MPS-A55.
 - DIODES ARE 1N456.
 - RESISTOR VALUES ARE 5% TOLERANCE UNLESS OTHERWISE SPECIFIED.
 - ALL ELECTROLYTICS ARE 20% TOLERANCE UNLESS OTHERWISE SPECIFIED.
 - LOADING CAPACITOR VALUES DEPEND ON THE LOAD OF THE FOLLOWING GROUP.
 - 10% CAP - C6, C20, C34, C43.
 - 5% CAPS - C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C35, C36, C37, C38, C39, C40, C41, C42, C44, C45, C46, C47, C48, C49, C50, C51, C52.
 - 2% CAPS - C23, C25, C26, C27, C28, C29, C30, C31, C32, C33, C35, C36, C37, C38, C39, C40, C41, C42, C44, C45, C46, C47, C48, C49, C50, C51, C52.
 - RESISTOR VALUES ARE 5% TOLERANCE UNLESS OTHERWISE SPECIFIED.
 - ADJUST RESISTOR R13 SO THAT Q4 IS CONDUCTING AT 100 KHZ. WITH LTR05 AND RTR04C4 SHOULD BE CUT-OFF.
 - Q10 AND Q12 ARE MPS-A65.
 - POWER SUPPLY = 20-20-20 MA.

SEE NOTE 7
 0 LF OUTPUT
 SEE NOTE 7

SEE NOTE 7
 0 RB OUTPUT
 SEE NOTE 7

SEE NOTE 7
 0 LB OUTPUT
 SEE NOTE 7

50 LOGIC DECODER, L-3, DWG. NO. 4035A, REV. A

REF. DWG. P.C. 4035A 403578

A Division of Columbia Broadcasting System, Inc.
51 West 52 Street
New York, N. Y. 10019
(212) 765-4321

FOR
BOOKS
K.A. Electronics

Mr. Glenney

Dear SQ Licensee: .

March 13, 1974

In January you received "preliminary" specifications and design schematics for three SQTM logic circuit options. We can now provide you with revised recommended circuit schematics and specifications for the SQ logic IC system. These SQ Logic circuit options, described in the attached technical bulletin, enable an audio manufacturer to use SQ logic in either the most sophisticated audio equipment or in budget priced units without sacrifices in listening quality. The design engineer's choice will depend on the technical and cost requirements of the particular quadrasonic product.

We are also pleased to point out that our design engineers have been able to greatly enhance the logic performance specifications for all three circuit options without additional cost to the manufacturer. These improvements include the separation and distortion figures.

If you have any questions covering the data call Emil Torick or Dan Gravereaux at CBS Laboratories (Area Code 203 327-2000) for consultation.

Motorola's SQ logic ICs are shipping to manufacturers. If you need special assistance relative to IC samples or production orders we recommend that you contact Mr. Mel Downs at Motorola Semiconductor, Phoenix, Arizona (602-962-3253).

Cordially,

Joseph F. Dash
Joseph F. Dash
Director Diversification

P.S. You will be interested in the attached brochure describing SONY's convenient and low cost SQE-2000 encoder which provides electronic signal sources for testing and alignment of decoders.

SQ is a trademark of Columbia Broadcasting System, Inc.

Regards

Jim Freed

SQ™ LOGIC DECODER DESIGNS
(REVISED)

Each full logic decoder, L1, L2, and L3, has been revised to take advantage of the Motorola production IC characteristics and to bring the best quadraphonic performance to consumer products.

The improvements implemented since our mailing of January 4th are:

L1

- The back channel separation is increased to 12 dB.
- The AGC feedback circuit (Pin 11 on the 1315) is now more responsive to program average waveforms, increasing the range of logic control especially for transient-type sounds.
- The main VCA time-constant capacitors have been increased for better logic stability and improved operation with the modified AGC.

L2

- Back channel separation is increased to 15 dB.
- The improvements to the AGC and VCA time-constants are identical to L1.
- Variable blend has been reduced in complexity and scope. Inasmuch as center-back is a rarely used position, the front channel variable blend FET has been removed. The performance remains excellent for center-front sounds, with improvement in the constant power requirement of logic.

L3

- Similar to L2, the back channel separation is now 15 dB and the AGC and VCA changes are identical to L1 and L2.
- The variable blend is improved according the L2.
- The discrete component 8-pole matrix portion now includes emitter follower phase shift drivers to take full advantage of the phase accuracy available with precision RC values. Its performance is now exceptional, having low distortion, high overload capability, and excellent phase accuracy.

March 1974

SQ™ DECODERS USING MC1312, 1314, and 1315 IC'S

TYPICAL PERFORMANCE SPECIFICATIONS

TYPE	COMPONENTS	APPROX. RELATIVE COST (1)	TYPICAL SEPARATION IN dB (2)	SUGGESTED CBS SCHEMATIC NO.	TYPICAL PERFORMANCE SPECIFICATIONS	IC SOURCES	GENERAL DESCRIPTION & SUGGESTED APPLICATION
L-1 Basic IC logic, wave-matching & front-back logic	(3) MC1312 MC1314 MC1315 23 resistors 37 capacitors	\$12		403654B	Logic controlled output level vs frequency: ±1 dB, 50 Hz - 15 kHz (center-front, 50 Hz - 6 kHz) Distortion: THD 0.5%, 50 Hz - 20 kHz	MOT. (4)	L-1 is a full logic decoder minimum cost and complexity suitable for moderate cost systems and components
L-2 Wave-matching & variable-blend	MC1312 MC1314 MC1315 41 resistors 39 capacitors 9 transistors 6 diodes 1 potentiometer	\$13		403627D	Logic controlled output level vs frequency: ±1 dB, 50 Hz - 15 kHz (center-front, 30 Hz - 10 kHz) Distortion: THD 0.5%, 50 Hz - 20 kHz	MOT. (4)	L-2 is a more advanced full-logic decoder exhibiting improved back, and front-back separation suitable for high priced integrated music syst and components.
L-3 Wave-matching & variable-blend --8-pole discrete component matrix	MC1314 MC1315 100 resistors 55 capacitors 21 transistors 6 diodes 1 potentiometer	\$14		403656A	Logic controlled output level vs frequency: ±1 dB, 25 Hz - 20 kHz Distortion: THD 0.5%, 30 Hz - 20 kHz	MOT. (4)	L-3 is a superior full-logic decoder featuring high precision 8-pole phase-shift networks (MC1312 not used) with high fidelity specifications suitable for "top-of-the-line" equipment
M-1 Basic matrix with fixed 10-40 blend	MC1312 8 resistors 10 capacitors	\$3		403657	Frequency response: ±1 dB, 50 Hz - 15 kHz Distortion: THD 0.25%, 20 Hz - 20 kHz	MOT. (4)	M-1 is the basic SQ Matrix decoder with "10-40" blend without logic capability. Intended for use in inexpensive equipment

(1) Cost will vary with purchased parts quantities

(2) With maximum dimension control setting

(3) "MC" refers to Motorola Semiconductor IC's

(4) Also Fairchild Semiconductor in late 1974

VARIABLE BLEND

SQ FULL LOGIC DECODER USING MOTOROLA INTEGRATED CIRCUITS

The blending technique is being used in SQ matrix decoders to increase the center-front to center-back separation. Blending combines a portion of the left-back signal with the right-back signal and vice versa. Since a center-front signal appears out-of-phase at the two back terminals of the SQ matrix decoder, blending causes this signal to subtract (decrease) in the backs. The result is an increase in center-front to center-back separation while the left to right separation in the back is slightly decreased.

The blend function can be made variable according to the time varying requirements during musical program interplay. In the absence of either a center-front or a center-back sound, the blend is basically off permitting full left to right separation. For either a center-front or a center-back sound, the blend is actuated causing the front-to-back separation to rapidly increase. Following the event, the blend releases "slowly" within 50 milliseconds.

The variable-blend circuit can be easily incorporated into the integrated circuit full logic SQ decoder L2, as shown by the schematic, No. 403627D.

The variable-blend function is implemented by a field-effect transistor (FET), acting as variable resistor. It is connected across the two back matrix outputs. Control signal for the FET is derived from the logic IC (MC-1315).

Since the original front-back logic associated with the variable gain amplifiers must be inhibited in the logic IC, an external swamping resistor is used to reduce this logic voltage at the IC terminals to a value below the operating threshold within this IC. The voltage at these terminals still represents the front-back logic and is, therefore, amplified and used to control the FET resistance.

In general, there are only two states associated with a FET; a high resistance ($>1.5M\Omega$) and a low resistance ($<300\Omega$) state. In the decoder a fixed resistor in parallel with the FET gives a 20% blend. When the FET is at a low resistance, the back channel blend changes

to 70%. In this condition, a center-front sound will have a front to back separation of 18 dB. The back corner sounds will have only a slight level variation.

Referring to the schematic diagram, there are four emitter followers (Q1, Q2, Q3, Q4) isolating the matrix IC (MC-1312) from the variable-gain IC (MC-1314). Q5 blends, under actuation, the two back channel currents as defined by the $2K\Omega$ series resistors and the 750Ω shunt resistor. The low resistance state of the FET contributes also to the shunt resistance value.

A $2.7K\Omega$ resistor, connected between Pins 7 and 8 on the logic IC (MC-1315), inhibits its front/back logic actuation. These voltages are then fed, via the required smoothing circuits ($1K\Omega$, $3\mu F$), to the two bases of a differential amplifier (Q7, Q8). The common mode DC voltages at Pins 7 and 8 (~ 11 VDC) produce no differential output at the collectors of Q7 and Q8. When the logic indicates either a center-front or a center-back signal, one collector will forward bias its diode causing the FET driver transistor Q9 to conduct.

Q9 is normally not conducting, thereby placing the full supply voltage (20V) on the FET gate. The FET appears as an open circuit. When Q9 conducts, a saturated state is reached, causing the FET gate voltage to drop close to ground (1 volt or so) and thereby reducing the FET impedance to a low-value ($100-300\Omega$).

A constant current source Q10 is needed to stabilize the operating point of the differential amplifier for variations in both the common-mode voltage at Pins 7 and 8 of the IC and for temperature variations. The 100Ω rheostat in the emitter of Q10 directly controls the operating point of both Q7 and Q8.

The rheostat must be adjusted to provide the proper blend action for musical sounds which have been encoded as center-front. In fact, the FET blend acts as a switch and must be actuated whenever a signal is moved from, say left-front towards center front.

A method for adjusting the rheostat is as follows:

1. Connect a high impedance DC voltmeter to the FET gates control line.
2. Adjust the rheostat so that the gate voltage is near 20 V DC (Q9 not conducting and blend is off).
3. Apply 1 kHz sine wave to L_p at operating level (0.5 V rms) and make sure that Q9 remains in the non-conducting state.

4. Apply the same 1 kHz, in phase, to R_T at a level of 0.08 V rms.
5. Turn the rheostat so that the FET gate voltage just changes to around 1 V DC (See that Q9 is fully conducting and a blend is actuated).
6. Make sure that the blend releases for $R_T = 0.05$ V rms, and is fully actuated for $R_T = 0.11$ V rms. The variable blend function is now optimum for center-front dynamic separation.

D. W. Gravereaux

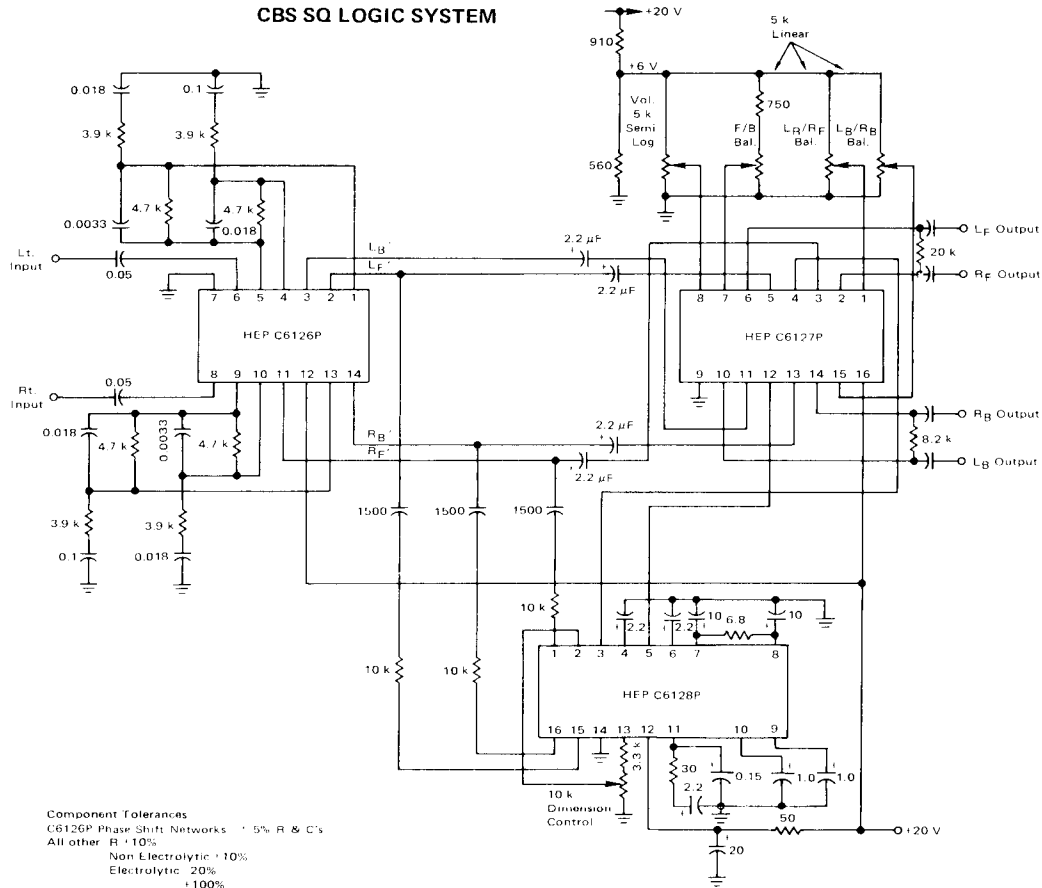
March 4, 1974



FOUR CHANNEL SQ* LOGIC DECODER SYSTEM



CBS SQ LOGIC SYSTEM



Component Tolerances
 C6126P Phase Shift Networks ± 5% R & C's
 All other R ± 10%
 Non Electrolytic ± 10%
 Electrolytic 20%
 ± 100%

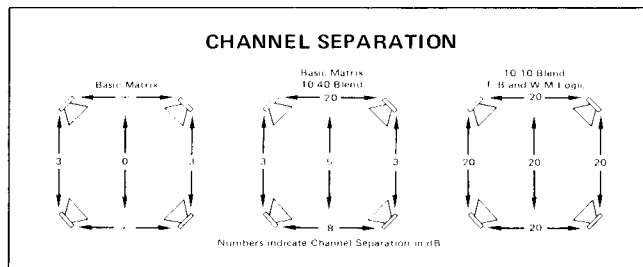
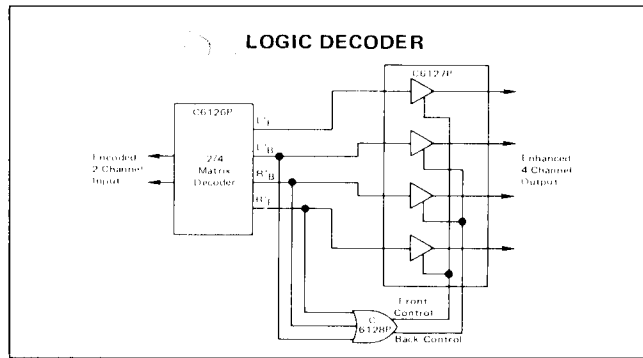
WHY LOGIC?

Enhances front to back separation from 6 dB to 20 dB.

Front-to-back separation of SQ material can be enhanced by the C6128P logic circuit which detects the presence of dominant front or back signals and adjusts the front-back gain relationship of the C6127P to enhance the relative gain of the dominant channels.

Front and back control voltages (from the C6128P) are connected to the C6127P. Although the relative gains of the front and back channels are altered with these control signals, they vary in a complementary manner to maintain constant power output from the C6127P.

*Trademark of Columbia Broadcasting Systems, Inc.



Circuit diagrams external to Motorola products are shown as a means of illustrating typical semiconductor applications; consequently, complete information sufficient for construction purposes is not necessarily given. The information contained herein has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Motorola Inc. or others.



TYPICAL SYSTEM PERFORMANCE CHARACTERISTICS (C6126P, C6127P, C6128P)

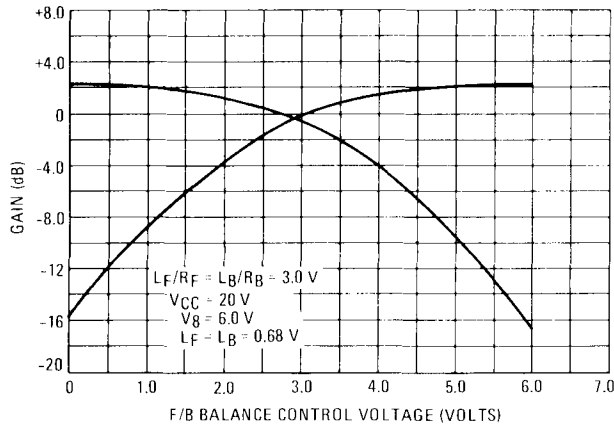
Power Supply Requirements: 60 mA at 20 V Nominal Signal Level: 0.5 V Maximum Input Voltage: 1.9 V Input Impedance: 2 M Ω Output Impedance: 2 k Ω	Total Harmonic Distortion: 0.2% at nominal input at 1 Hz Voltage Gain (at quiescent): 1.0 4 Channel Volume Control: Range - 70 dB; Tracking - within 3 dB 4 Channel Balance Control: -35 dB at -20 dB gain
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NOTES

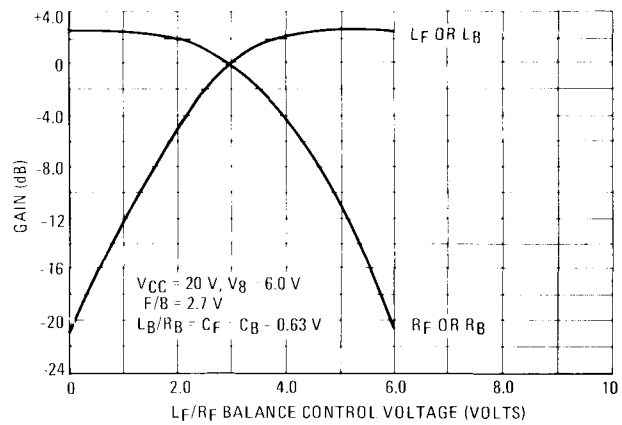
<p>C6127P</p> <ol style="list-style-type: none"> If volume control is not used, connect Pin 8 to +6.0 V. If balance controls are not used, open Pins 1, 7 and 15. L_F/R_F and L_B/R_B balance controls can be ganged by connecting Pins 1 and 15. Signal handling capability is reduced at maximum logic (20 dB front to back separation) unless V_{CC} = 25 V on C6127P. <p>C6128P</p> <ol style="list-style-type: none"> The logic control will provide enhancement of front to back separation from 6 dB typical to 20 dB max (15 dB typical at the recommended operating level of 50% control). To defeat the logic use the circuit connections as shown on right. 	<p style="text-align: right;">To pins 4 and 12 MC1314</p>
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SYSTEM CHARACTERISTICS

GAIN versus F/B BALANCE



GAIN versus L_F/R_F BALANCE CONTROL



CBS LOGIC SYSTEM WITH VARIABLE BLEND

