COMPANDOR NE570/571/SA571

DESCRIPTION

The NE570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The NE570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

CIRCUIT DESCRIPTION

The NE570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|\ \text{ave}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|\ \text{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\quad \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

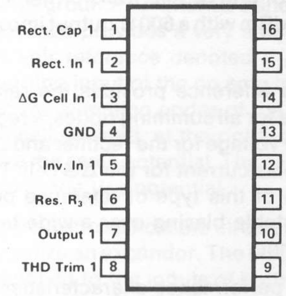
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components.

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

PIN CONFIGURATION

F, N PACKAGE

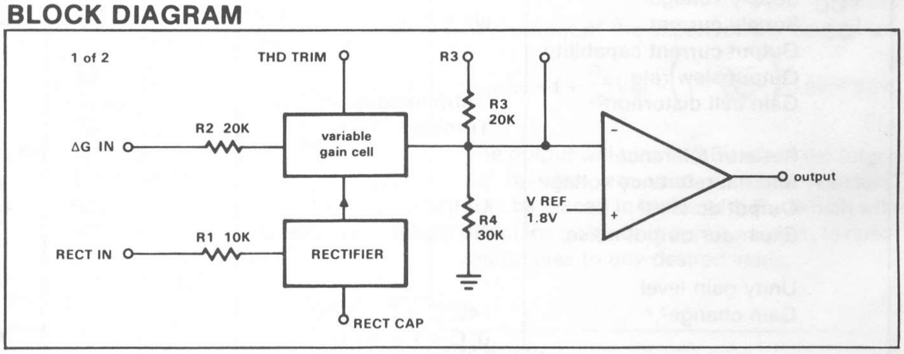


Order Part No.
NE570 F,N
NE571 F,N
SA571 F,N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range		
	NE	0 to 70	°C
	SA	-40 to +85	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



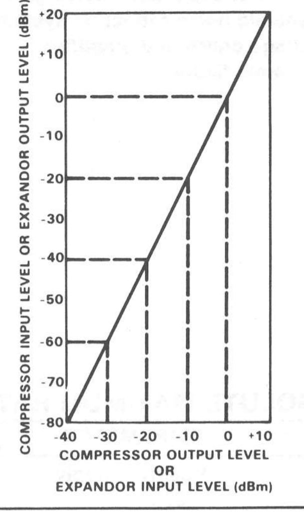
The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600 Ω output impedance.

A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

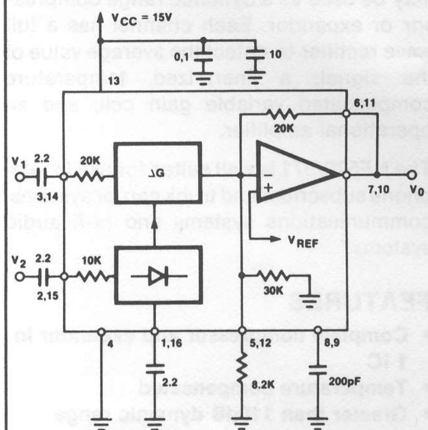
The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS

BASIC INPUT-OUTPUT TRANSFER CURVE



TYPICAL TEST CIRCUIT



DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 15V[1]

PARAMETER	TEST CONDITIONS	NE570 Min	NE570 Typ	NE570 Max	NE/SA571[6] Min	NE/SA571[6] Typ	NE/SA571[6] Max	UNIT
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0		3.2	4.8	mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					μV
			−15					dBRNC
Unity gain level		−1	0	+1	−1.5	0	+1.5	dBm
Gain change[2,4]	−40°C < T < 70°C		±.1			±.1		dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	−40°C < T < 70°C		+2, −25	−10, −40		+2, −25	+20, −50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	−40°C < T < 70°C		+8,−0					%
	0°C < T < 70°C		+1,−0					
Tracking error[5], input V_1 = OdBm	Rectifier input, V_2 =							dB
	+6dBm		±.2					
	−10dBm		+.2	−.2,+.4		+.2	−.2,+.5	
	−20dBm		+.2	−.3,+.6		+.2	−.4,+.7	
	−30dBm		+.2	−.5,+1		+.2	−1,+1.5	
	−40dBm		+.2,−.4			+.2,−.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm,1kHz
3. Expandor ac input change from no signal to OdBm
4. Relative to value at T_A = 25°C
5. Relative to OdBm
6. Electrical characteristics for the SA571 only are specified over -40 to +85°C temperature range.

INTRODUCTION

Much interest has been expressed in high performance electronic gain control circuits. For non-critical applications, an integrated circuit operational transconductance amplifier can be used, but when high performance is required, one has to resort to complex discrete circuitry with many expensive, well matched components. This paper describes a new integrated circuit, the NE570 Compandor, which offers a pair of high performance gain control circuits featuring low distortion (<.1%), high signal to noise ratio (90dB), and wide dynamic range (110dB).

CIRCUIT BACKGROUND

The NE570 Compandor was specifically designed to satisfy the requirements of the telephone system. When several telephone channels are multiplexed onto a common line, the resulting signal to noise ratio is poor and companding is used to allow a wider dynamic range to be passed through the channel. Figure 1 graphically shows what a compandor can do for the signal to noise ratio of a restricted dynamic range channel. The input level range of +20 to -80dB is shown undergoing a 2 to 1 compression where a 2dB input level change is compressed into a 1dB output level change by the compressor. The original 100dB of dynamic range is thus compressed to a 50dB range for transmission through a restricted dynamic range channel. A complementary expansion on the receiving end restores the original signal levels and reduces the channel noise by as much as 45dB.

The significant circuits in a compressor or expandor are the rectifier and the gain control element. The phone system requires a simple full wave averaging rectifier with good accuracy, since the rectifier accuracy determines the (input) output level tracking accuracy. The gain cell determines the distortion and noise characteristics, and the phone system specifications here are very loose. These specs could have been met with a simple operational transconductance multiplier, or OTA, but the gain of an OTA is proportional to temperature and this is very undesirable. Therefore, a linearized transconductance multiplier was designed which is insensitive to temperature and offers low noise and low distortion performance. It is hoped that these features will make the circuit as widely used in audio systems as it will be in telecommunications systems.

BASIC CIRCUIT HOOKUP AND OPERATION

Figure 2 shows the block diagram of one half of the chip, (there are two identical channels on the I.C.). The full wave averaging rectifier provides a gain control current, I_G, for the variable gain (ΔG) cell. The output of the ΔG cell is a current which is fed to the summing node of the operational amplifier. Resistors are provided to establish circuit gain and set the output dc bias.

RESTRICTED DYNAMIC RANGE CHANNEL

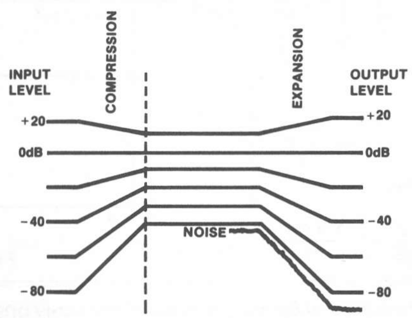


Figure 1

CHIP BLOCK DIAGRAM (1 OF 2 CHANNELS)

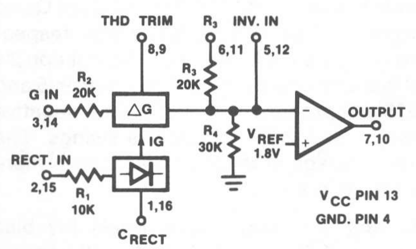


Figure 2

The circuit is intended for use in single power supply systems, so the internal summing nodes must be biased at some voltage above ground. An internal band gap voltage reference provides a very stable, low noise 1.8 volt reference denoted V_{ref}. The non-inverting input of the op amp is tied to V_{ref}, and the summing nodes of the rectifier and ΔG cell (located, at the right, of R_1 and R_2) have the same potential. The THD trim pin is also at the V_{ref} potential.

Figure 3 shows how the circuit is hooked up to realize an expandor. The input signal, V_{in}, is applied to the inputs of both the rectifier and the ΔG cell. When the input signal drops by 6dB, the gain control current will drop by a factor of 2, and so the gain will drop 6dB. The output level at V_{out} will thus drop 12dB, giving us the desired 2 to 1 expansion.

Figure 4 shows the hookup for a compressor. This is essentially an expandor placed in the feedback loop of the op amp. The ΔG cell is set up to provide ac feedback only, so a separate dc feedback loop is provided by the two R_{dc} and C_{dc}. The values of R_{dc} will determine the dc bias at the output of the op amp. The output will bias to:

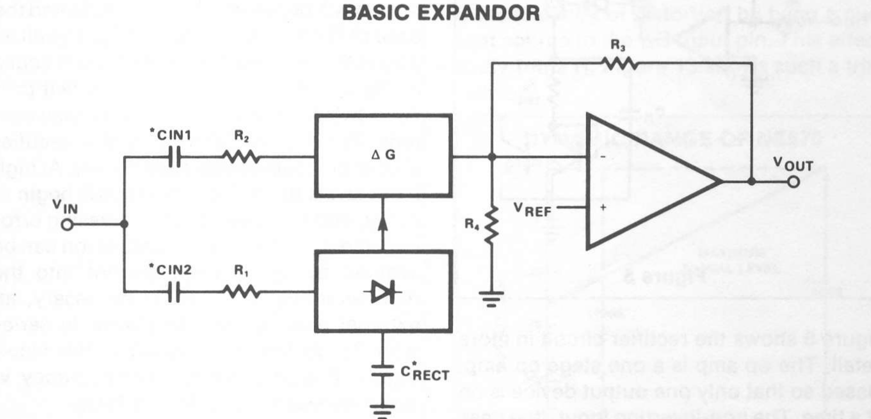
$$V_{out}\,dc = 1 + \frac{R_{dc1}+R_{dc2}}{R_4} V_{ref} = \left(1 + \frac{R_{dc\,tot}}{30K}\right) 1.8V$$

The output of the expandor will bias up to:

$$V_{out}\,dc = 1 + \frac{R_3}{R_4} V_{ref} = \left(1 + \frac{20K}{30K}\right) 1.8V = 3.0V$$

The output will bias to 3.0V when the internal resistors are used. External resistors may be placed in series with R_3, (which will affect the gain), or in parallel with R_4 to raise the dc bias to any desired value.

BASIC EXPANDOR



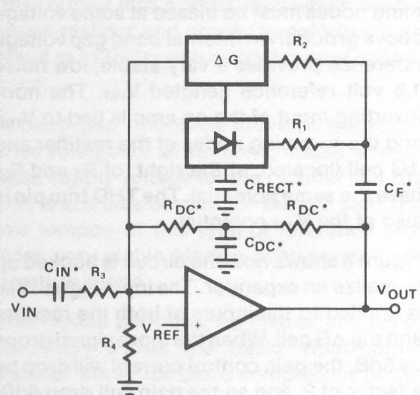
$$GAIN = \frac{2 R_3 V_{IN}\,(avg.)}{R_1 R_2 I_B}$$

$$I_B = 140\mu A$$

*external components

Figure 3

BASIC COMPRESSOR



$$GAIN = \left(\frac{R_1 R_2 I_B}{2 R_3 V_{IN}\,(avg.)}\right)^{1/2}$$

$I_B = 140\mu A$

*external components

Figure 4

CIRCUIT DETAILS-RECTIFIER

Figure 5 shows the concept behind the full wave averaging rectifier. The input current to the summing node of the op amp, V_{in}/R_1, is supplied by the output of the op amp. If we can mirror the op amp output current into a unipolar current, we will have an ideal rectifier. The output current is averaged by R_5, Cr, which set the averaging time constant, and then mirrored with a gain of 2 to become I_G, the gain control current.

RECTIFIER CONCEPT

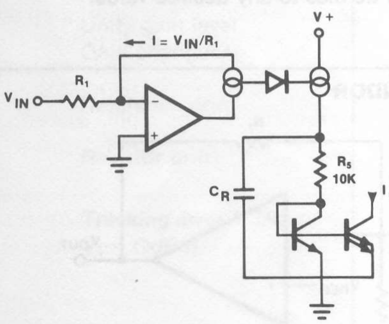
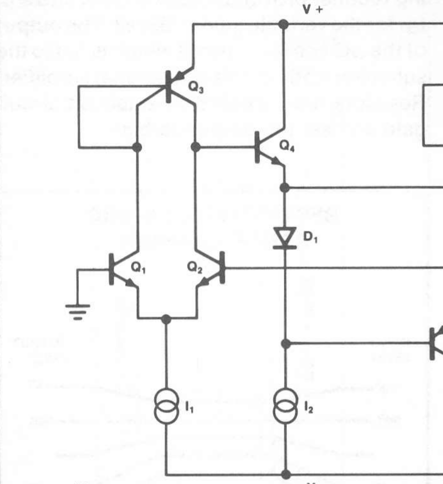


Figure 5

Figure 6 shows the rectifier circuit in more detail. The op amp is a one stage op amp, biased so that only one output device is on at a time. The non-inverting input, (the base of Q_1), which is shown grounded, is actually tied to the internal 1.8V V_{ref}. The inverting input is tied to the op amp output, (the emitters of Q_5 and Q_6), and the input summing resistor R_1. The single diode between the bases of Q_5 and Q_6 assures that only one device is on at a time. To detect the output current of the op amp, we simply use the collector currents of the output devices Q_5 and Q_6. Q_6 will conduct when the input swings positive and Q_5 conducts when the input swings negative. The collector currents will be in error by the α of Q_5 or Q_6 on negative or positive signal swings, respectively. IC's such as this have typical npn β's of 200 and pnp β's of 40. The α's of .995 and .975 will produce errors of .5% on negative swings and 2.5% on positive swings. The 1.5% average of these errors yields a mere .13dB gain error.

SIMPLIFIED RECTIFIER SCHEMATIC



$$I_G = 2\,\frac{V_{IN}\ avg.}{R1}$$

Figure 6

At very low input signal levels the bias current of Q_2, (typically 50nA), will become significant as it must be supplied by Q_5. Another low level error can be caused by dc coupling into the rectifier. If an offset voltage exists between the V_{in} input pin and the base of Q_2, an error current of V_{os}/R_1 will be generated. A mere 1mv of offset will cause an input current of 100na which will produce twice the error of the input bias current. For highest accuracy, the rectifier should be coupled into capacitively. At high input levels the β of the pnp Q_6 will begin to suffer, and there will be an increasing error until the circuit saturates. Saturation can be avoided by limiting the current into the rectifier input to 250μa. If necessary, an external resistor may be placed in series with R_1 to limit the current to this value. Figure 7 shows the rectifier accuracy vs input level at a frequency of 1kHz.

At very high frequencies, the response of the rectifier will fall off. The rolloff will be more pronounced at lower input levels due to the increasing amount of gain required to switch between Q_5 or Q_6 conducting. The rectifier frequency response for input levels of 0dBm, -20dBm, and -40dBm is shown in Figure 8. The response at all three levels is flat to well above the audio range.

RECTIFIER ACCURACY

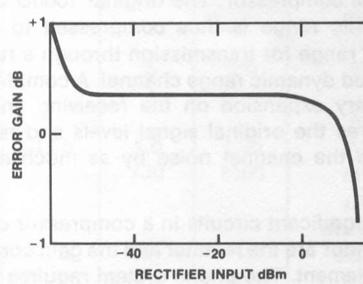


Figure 7

RECTIFIER FREQUENCY RESPONSE vs INPUT LEVEL

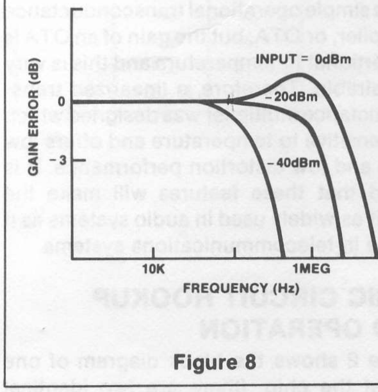


Figure 8

VARIABLE GAIN CELL

Figure 9 is a diagram of the variable gain cell. This is a linerarized two quadrant transconductance multiplier[1,2]. Q_1, Q_2 and the op amp provide a predistorted drive signal for the gain control pair, Q_3, Q_4. The gain is controlled by I_G and a current mirror provides the output current.

The op amp maintains the base and collector of Q_1 at ground potential (V_{ref}) by controlling the base of Q_2. The input current I_{in} ($= V_{in}/R_2$) is thus forced to flow through Q_1 along with the current I_1, so $I_{C1} = I_1 + I_{in}$. Since I_2 has been set at twice the value of I_1, the current through Q_2 is $I_2 - (I_1 + I_{in}) = I_1 - I_{in} = I_{C2}$. The op amp has thus forced a linear current swing between Q_1 and Q_2, by providing the proper drive to the base of Q_2. This drive signal will be linear for small signals, but very non-linear for large signals, since it is compensating for the nonlinearity of the differential pair Q_1, Q_2 under large signal conditions.

The key to the circuit is that this same predistorted drive signal is applied to the gain control pair Q_3 and Q_4. When two differential pairs of transistors have the same signal applied, their collector current ratios will be identical, regardless of the magnitude of the currents. This gives us:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{C4}}{I_{C3}} = \frac{I_1 + I_{in}}{I_1 - I_{in}}$$

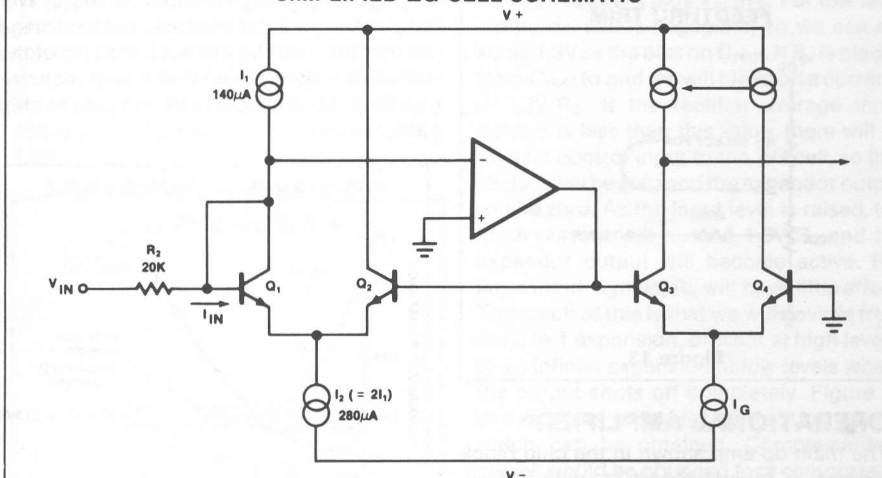
plus the relationships $I_G = I_{C3} + I_{C4}$ and $I_{out} = I_{C4} - I_{C3}$ will yield the multiplier transfer function,

$$I_{out} = \frac{I_G}{I_1} I_{in} = \frac{V_{in}}{R_2} \frac{I_G}{I_1}$$

this equation is linear and temperature insensitive, but it assumes ideal transistors.

If the transistors are not perfectly matched, a parabolic, non-linearity is generated, which results in 2nd harmonic distortion. Figure 10 gives an indication of the maginitude of the distortion caused by a given input level and offset voltage. The distortion is linearly proportional to the magnitude of the offset and the input level. Saturation of the gain cell occurs at a +8dBm level. At a nominal operating level of 0dBm, a 1mv offset will yield .34% of second harmonic distortion. Most circuits are somewhat better than this, which means our overall offsets are typically about 1/2mv. The distortion is not affected by the magnitude of the gain control current, and it does not increase as the gain is changed. This second harmonic distortion could be eliminated by making perfect transistors, but since that would be difficult, we have had to resort to other methods. A trim pin has been provided to allow trimming of the internal offsets to zero, which effectively eliminated second harmonic distortion. Figure 11 shows the simple trim network required.

SIMPLIFIED ΔG CELL SCHEMATIC



$$I_{OUT} = \frac{I_G}{I_1} I_{IN} = \frac{I_G V_{IN}}{I_2 R_2}$$

Figure 9

ΔG CELL DISTORTION vs OFFSET VOLTAGE

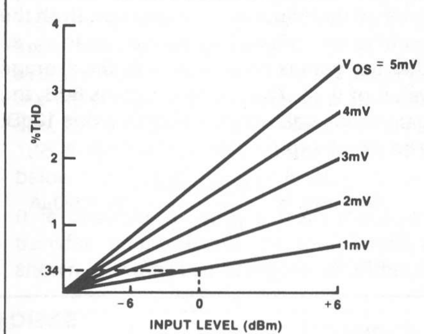


Figure 10

THD TRIM NETWORK

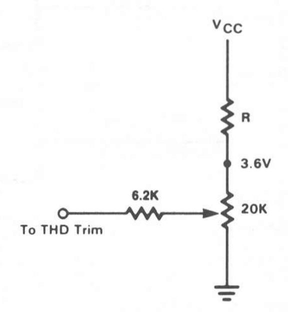


Figure 11

Figure 12 shows the noise performance of the ΔG cell. The maximum output level before clipping occurs in the gain cell is plotted along with the output noise in a 20kHz bandwidth. Note that the noise drops as the gain is reduced for the first 20dB of gain reduction. At high gains, the signal to noise ratio is 90dB, and the total dynamic range from maximum signal to minimum noise is 110dB.

Control signal feed-through is generated in the gain cell by imperfect device matching and mismatches in the current sources I_1 and I_2. When no input signal is present, changing I_G will cause a small output signal. The distortion trim is effective in nulling out any control signal feed-through, but in general, the null for minimum feed-through will be different than the null in distortion. The control signal feed-through can be trimmed independently of distortion by tying a current source to the ΔG input pin. This effectively trims I_1. Figure 13 shows such a trim network.

DYNAMIC RANGE OF NE570

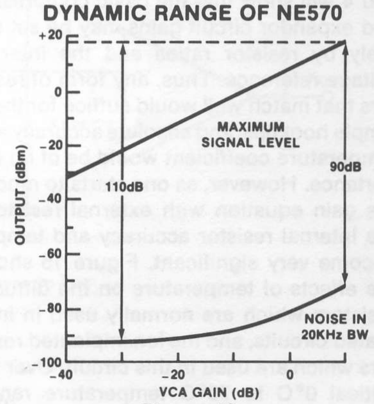


Figure 12

CONTROL SIGNAL FEEDTHRU TRIM

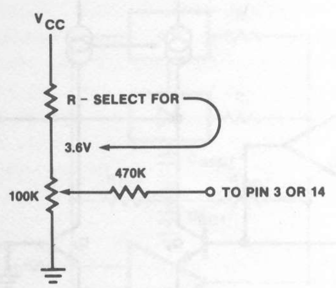


Figure 13

OPERATIONAL AMPLIFIER

The main op amp shown in the chip block diagram is equivalent to a 741 with a 1MHz bandwidth. Figure 14 shows the basic circuit. Split collectors are used in the input pair to reduce g_m, so that a small compensation capacitor of just 10pf may be used. The output stage, although capable of output currents in excess of 20ma., is biased for a low quiescent current to conserve power. When driving heavy loads, this leads to a small amount of crossover distortion.

OPERATIONAL AMPLIFIER

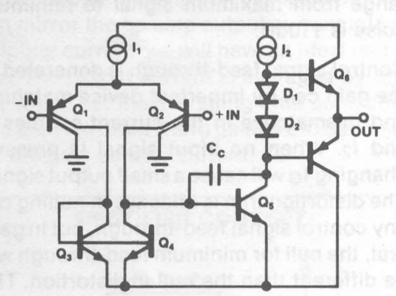


Figure 14

RESISTORS

Inspection of the gain equations in Figure 3 and 4 will show that the basic compressor and expandor circuit gains may be set entirely by resistor ratios and the internal voltage reference. Thus, any form of resistors that match well would suffice for these simple hookups, and absolute accuracy and temperature coefficient would be of no importance. However, as one starts to modify the gain equation with external resistors, the internal resistor accuracy and tempco become very significant. Figure 15 shows the effects of temperature on the diffused resistors which are normally used in integrated circuits, and the ion implanted resistors which are used in this circuit. Over the critical 0°C to 70°C temperature range, there is a 10 to 1 improvement in drift from a 5% change for the diffused resistors, to a .5% change for the implemented resistors. The implanted resistors have another advantage in that they can be made 1/7 the size of the diffused resistors due to the higher resistivity. This saves a significant amount of chip area.

RESISTANCE vs TEMPERATURE

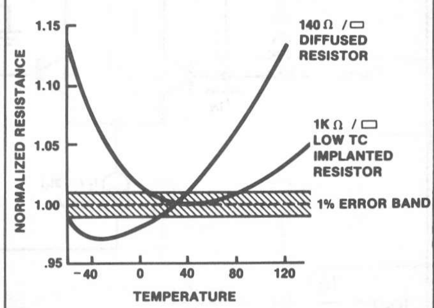


Figure 15

APPLICATIONS

The following circuits will illustrate some of the wide variety of applications for the NE570.

BASIC EXPANDOR

Figure 16 shows how the circuit would be hooked up for use as an expandor. Both the rectifier and ΔG cell inputs are tied to V_{in} so that the gain is proportional to the average value of (V_{in}). Thus, when V_{in} falls 6dB, the gain drops 6dB and the output drops 12dB. The exact expression for the gain is

$$\text{Gain exp.} = \frac{2\, R_3\, V_{in}\ (\text{ave})}{R_1\, R_2\, I_B}\ ;\ I_B = 140\mu A$$

The maximum input that can be handled by the circuit in Figure 16 is a peak of 3V. The rectifier input current can be as large as $I = 3V/R_1 = 3V/10K = 300\mu A$. The ΔG cell input current should be limited to $I = 2.8V/R_2 = 2.8V/20K = 140\mu A$. If it is necessary to handle larger input voltages than $0 \pm 2.8V$ pk, external resistors should be placed in series with R_1 and R_2 to limit the input current to the above values.

Figure 16 shows a pair of input capacitors C_{in1} and C_{in2}. It is not necessary to use both capacitors if low level tracking accuracy is not important. If R_1 and R_2 are tied together and share a common capacitor, a small current will flow between the ΔG cell summing node and the rectifier summing node due to offset voltages. This current will produce an error in the gain control signal at low levels, degrading tracking accuracy.

The output of the expandor is biased up to 3V by the dc gain provided by R_3, R_4. The output will bias up to

$$V_{out}\ dc = \left(1 + \frac{R_3}{R_4}\right) V_{ref}$$

For supply voltages higher than 6V, R_4 can be shunted with an external resistor to bias the output up to $1/2 V_{CC}$.

Note that it is possible to externally increase R_1, R_2, and R_3, and to decrease R_3 and R_4. This allows a great deal of flexibility in setting up system levels. If larger input signals are to be handled, R_1 and R_2 may be increased; if a larger output is required, R_3 may be increased. To obtain the largest dynamic range out of this circuit, the rectifier input should always be as large as possible (subject to the ±300μA peak current restriction).

BASIC EXPANDOR

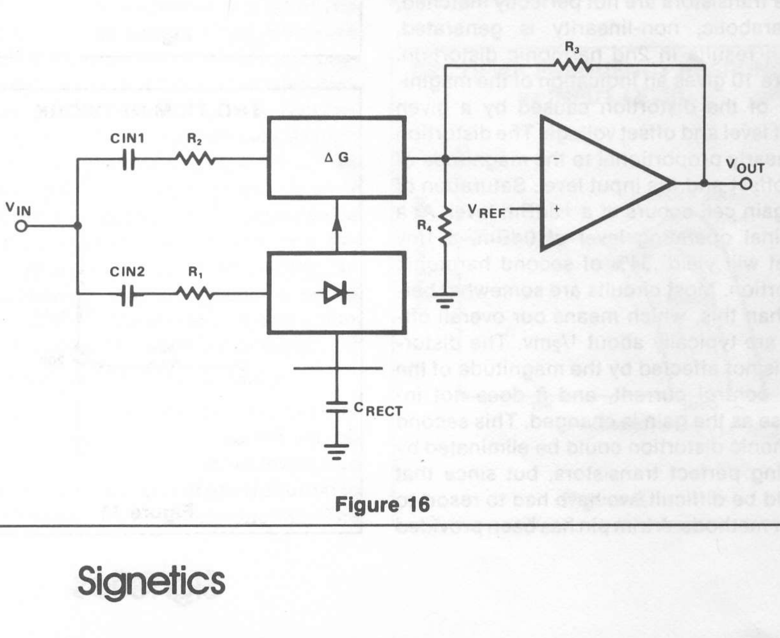


Figure 16

BASIC COMPRESSOR

Figure 17 shows how to use the NE570/571 as a compressor. It functions as an expandor in the feedback loop of an op amp. If the input rises 6dB, the output can rise only 3dB. The 3dB increase in output level produces a 3dB increase in gain in the ΔG cell, yielding a 6dB increase in feedback current to the summing node. Exact expression for gain is

$$\text{Gain comp.} = \left[\frac{R_1 R_2 I_B}{2 R_3 V_{in}\ (ave)}\right]^{1/2}$$

BASIC COMPRESSOR

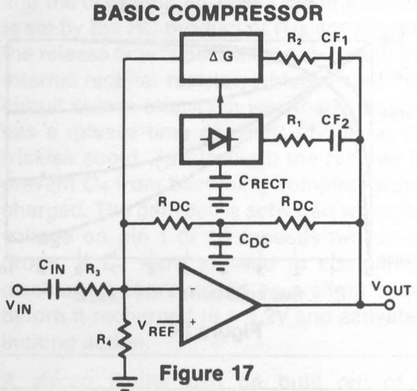


Figure 17

The same restrictions for the rectifier and ΔG cell maximum input current still hold, which place a limit on the maximum compressor output. As in the expandor, the rectifier and ΔG cell inputs could be made common to save a capacitor, but low level tracking accuracy would suffer. Since there is no dc feedback path around the op amp through the ΔG cell, one must be provided externally. The pair of resistors R_{dc} and the capacitor C_{dc} must be provided. The op amp output will bias up to

$$V_{out}\ dc = \left(1 + \frac{2 R_{dc}}{R_4}\right) V_{ref}$$

For the largest dynamic range, the compressor output should be as large as possible so that the rectifier input is as large as possible (subject to the ±300μA peak current restriction). If the input signal is small, a large output can be produced by reducing R_3 with the attendant decrease in input impedance, or by increasing R_1 or R_2. It would be best to increase R_2 rather than R_1 so that the rectifier input current is not reduced.

DISTORTION TRIM

Distortion can be produced by voltage offsets in the ΔG cell. The distortion is mainly even harmonics, and drops with decreasing input signal. (Input signal meaning the current into the ΔG cell.) The THD trim terminal provides a means for trimming out the offset voltages and thus trimming out the distortion. The circuit shown in Figure 18 is suitable, as would be any other capable of delivering ±30μA into 100Ω resistor tied to 1.8V.

THD TRIM NETWORK

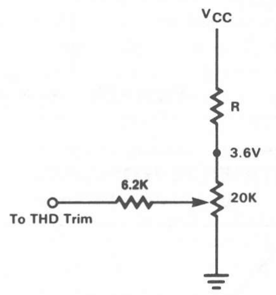


Figure 18

LOW LEVEL MISTRACKING

The compandor will follow a 2 to 1 tracking ratio down to very low levels. The rectifier is responsible for errors in gain, and it is the rectifier input bias current of <100na that produces errors at low levels. The magnitude of the error can be estimated. For a full scale rectifier input signal of ±200μA, the average input current will be 127μA. When the input signal level drops to a 1μA average, the bias current will produce a 10% or 1dB error in gain. This will occur at 42dB below the maximum input level.

It is possible to deviate from the 2 to 1 transfer characteristic at low levels as shown in the circuit of Figure 19. Either R_a or R_b, (but not both), is required. The voltage on C_{rect} is $2xV_{be}$ plus V_{in} ave. For low level inputs V_{in} ave is negligible, so we can assume 1.3V as the bias on C_{rect}. If R_a is placed from C_{rect} to gnd we will bleed off a current $I = 1.3V/R_a$. If the rectifier average input current is less than this value, there will be no gain control input to the ΔG cell, so that its gain will be zero and the expandor output will be zero. As the input level is raised, the input current will exceed $1.3V/R_a$ and the expandor output will become active. For large input signals, R_a will have little effect. The result of this is that we will deviate from the 2 to 1 expansion, present at high levels, to an infinite expansion at low levels where the output shuts off completely. Figure 20 shows some examples of tracking curves which can be obtained. Complementary curves would be obtained for a compressor, where at low level signals the result would be infinite compression. The bleed current through R_a will be a function of temperature because of the two V_{be} drops, so the low level tracking will drift with temperature. If a negative supply is available, it would be desirable to tie R_a to that, rather than ground, and to increase its value accordingly. The bleed current will then be less sensitive to the V_{be} temperature drift.

R_b will supply an extra current to the rectifier equal to $(V_{CC} - 1.3V)/R_b$. In this case, the expandor transfer characteristic will deviate towards 1 to 1 at low levels. At low levels the expandor gain will stop dropping and the expansion will cease. In a compressor this would lead to a lack of compression at low levels. Figure 21 shows some typical transfer curves. An R_b value of approximately 2.5Meg would trim the low level tracking so as to match the Bell system N2 trunk compandor characteristic.

EXPANDOR WITH LOW LEVEL MISTRACKING

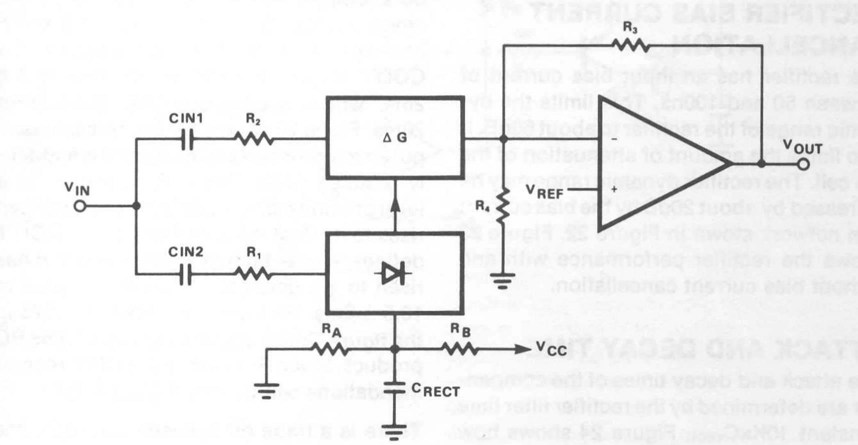


Figure 19

MISTRACKING WITH R_A

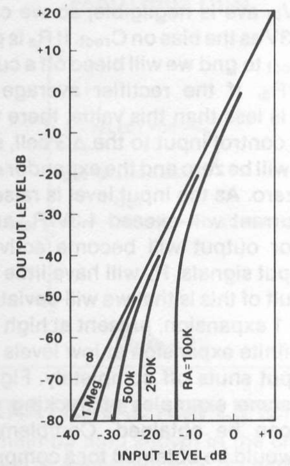


Figure 20

MISTRACKING WITH R_B

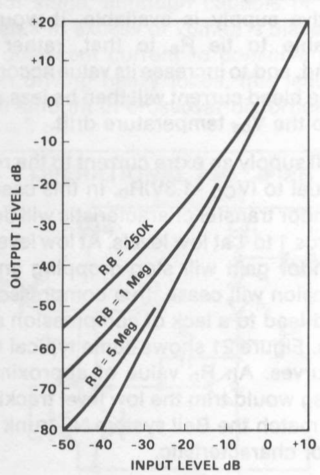


Figure 21

RECTIFIER BIAS CURRENT CANCELLATION

The rectifier has an input bias current of between 50 and 100na. This limits the dynamic range of the rectifier to about 60dB. It also limits the amount of attenuation of the ΔG cell. The rectifier dynamic range may be increased by about 20dB by the bias current trim network stown in Figure 22. Figure 23 shows the rectifier performance with and without bias current cancellation.

ATTACK AND DECAY TIME

The attack and decay times of the compandor are determined by the rectifier filter time constant $10K \times C_{rect}$. Figure 24 shows how the gain will change when the input signal undergoes a 10, 20, or 30dB change in level. The attack time is much faster than the decay, which is desirable in most applications. Figure 25 shows the compressor attack envelope for a +12dB step in input level. The initial output level of 1 unit instantaneously rises to 4 units, and then starts to fall towards its final value of 2 units. The CCITT recommendation on attack and decay times for telephone system compandors, defines the attack time as when the envelope has fallen to a level of 3 units, corresponding to t = .15 in the figure. The CCITT recommends an attack time of 3 ± 2ms, which suggests an RC product of 20ms. Figue 26 shows the compressor output envelope when the input level is suddenly reduced 12dB. The output, initially at a level of 4 units, drops 12dB to 1 unit and then rises to its final value of 2 units. The CCITT defines release time as when the output has risen to 1.5 units, and suggests a value of 13.5 ± 9ms. This corresponds to t = .675 in the figure, which again suggests a 20ms RC product. Since R_1 = 10K, the CCITT recommendations will be met if $C_{rect} = 2\mu f$.

RECTIFIER BIAS CURRENT COMPENSATION

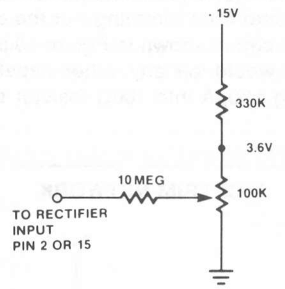


Figure 22

RECTIFIER PERFORMANCE WITH Ib COMPENSATION

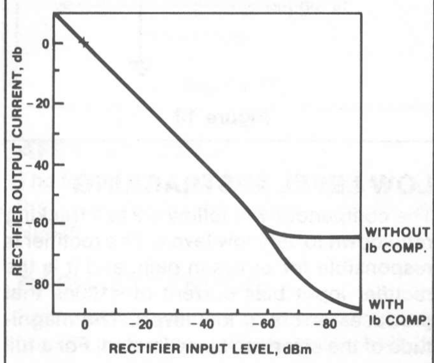


Figure 23

There is a trade off between fast response and low distortion. If a small C_{rect} is used to get very fast attack and decay, some ripple will appear on the gain control line and produce distortion. As a rule, a $1\mu f$ C_{rect} will produce .2% distortion at 1kHz. The distortion is inversely proportional to both frequency and capacitance. Thus, for telephone applications where $C_{rect} = 2\mu f$, the ripple would cause .1% distortion at 1kHz and .33% at 300hz. The low frequency distortion generated by a compressor would be cancelled (or undistorted) by an expandor, providing that they have the same value of C_{rect}.

GAIN vs TIME FOR INPUT STEPS OF ± 10, ± 20, ± 30dB

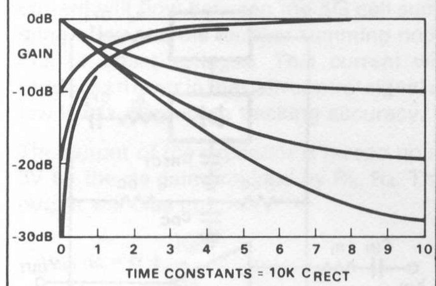


Figure 24

COMPRESSOR ATTACK ENVELOPE +12dB STEP

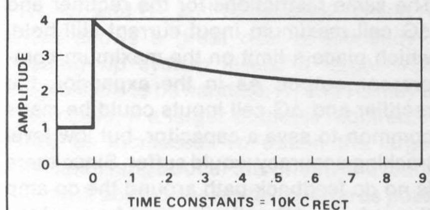


Figure 25

COMPRESSOR RELEASE ENVELOPE -12dB STEP

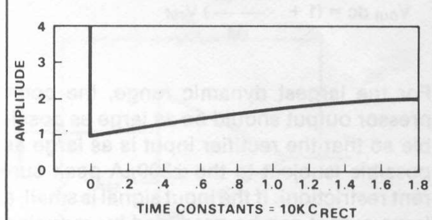


Figure 26

FAST ATTACK, SLOW RELEASE HARD LIMITER

The NE570/571 can be easily used to make an excellent limiter. Figure 27 shows a typical circuit which requires 1/2 of an NE570/571, 1/2 of an LM339 quad comparator, and a pnp transistor. For small signals, the ΔG cell is nearly off, and the circuit runs at unity gain as set by R_8, R_7. When the output signal tries to exceed a + or − 1 volt peak, a comparator threshold is exceeded. The pnp is turned on and rapidly charges C_4 which activates the ΔG cell. Negative feedback through the ΔG cell reduces the gain, and the output signal level. The attack time is set by the RC product of R_{18} and C_4, and the release time is determined by C_4 and the internal rectifier resistor, which is 10K. The circuit shown attacks in less than 1ms and has a release time constant of 100ms. R_9 trickles about .7μA through the rectifier to prevent C_4 from becoming completely discharged. The gain cell is activated when the voltage on pin 1 or 16 exceeds two diode drops. If C_4 were allowed to completely discharged, there would be a slight delay before it recharged to > 1.2V and activated limiting action.

A stereo limiter can be built out of 1 NE570/571, 1 LM339 and two pnp transistors. The resistor networks R_{12}, R_{13} and R_{14}, R_{15}, which set the limiting thresholds, could be common between channels. To gang the stereo channels together (limiting in one channel will produce a corresponding gain change in the second channel to maintain the balance of the stereo image), then pins 1 and 16 should be jumpered together. The outputs of all 4 comparators may then be tied together, and only one pnp transistor and one capacitor C_4 need be used. The release time will then be the product 5KxC4 since two channels are being supplied current from C_4.

USE OF EXTERNAL OP AMP

The operational amplifiers in the NE570/571 is not adequate for some applications. The slew rate, bandwidth, noise, and output drive capability can limit performance in many systems. For best performance, an external op amp can be used. The external op amp may be powered by bipolar supplies for a larger output swing.

Figure 28 shows how an external op amp may be connected. The non-inverting input must be biased at about 1.8V. This is easily accomplished by tying it to either pin 8 or 9, the THD trim pins, since these pins sit at 1.8V. An optional RC decoupling network is shown which will filter out the noise from the NE570/571 reference (typically about 10μv in 20kHz BW). The inverting input of the external op amp is tied to the inverting input of the internal op amp. The output of the external op amp is then used, with the internal op amp output left to float. If the external op amp is used single supply, (+V_{CC} and ground), it must have an input common mode range down to less than 1.8V.

USE OF EXTERNAL OP AMP

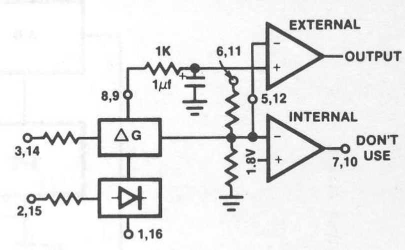


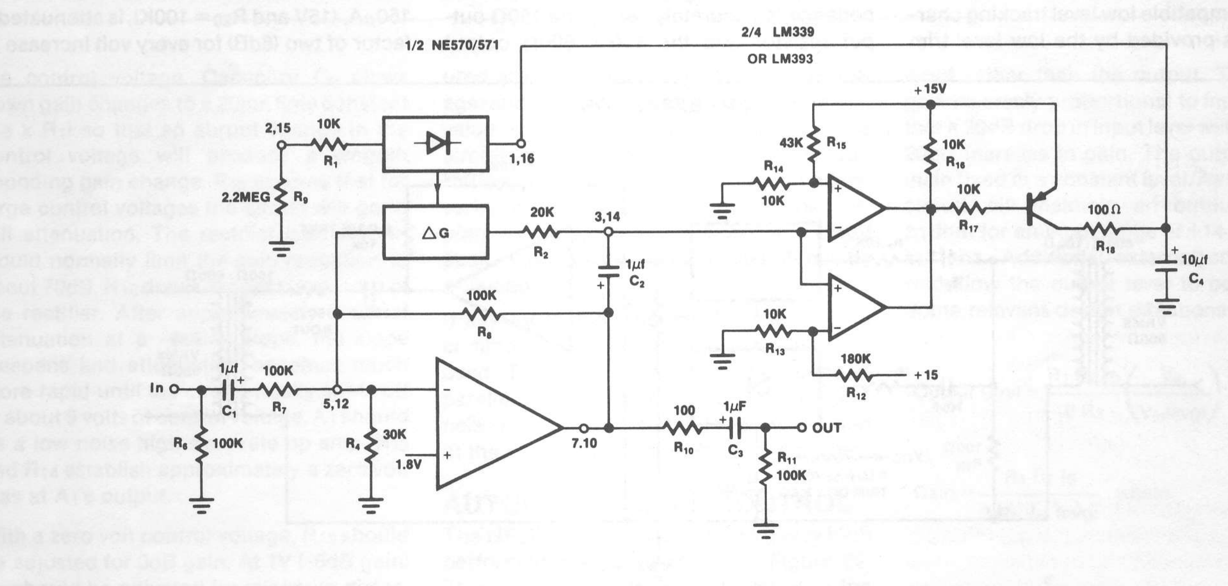
Figure 28

N2 COMPANDOR

There are four primary considerations involved in the application of the NE570/571 in an N2 compandor. These are matching of input and output levels, accurate 600Ω input and output impedances, conformance to the Bell system low level tracking curve, and proper attack and release times.

Figure 29 shows the implementation of an N2 compressor. The input level of .245V RMS is stepped up to 1.41V RMS by the 600Ω: 20KΩ matching transformer. The 20K input resistor properly terminates the transformer. An internal 20KΩ resistor (R_3) is provided, but for accurate impedance termination an external resistor should be used. The output impedance is provided by the 4K output resistor and the 4KΩ: 600Ω output transformer. The .275V RMS output level

FAST ATTACK, SLOW RELEASE HARD LIMITER



+15V Pin 13
GND Pin 4
R_1, R_2, R_4 are internal to the NE570/571.

Figure 27

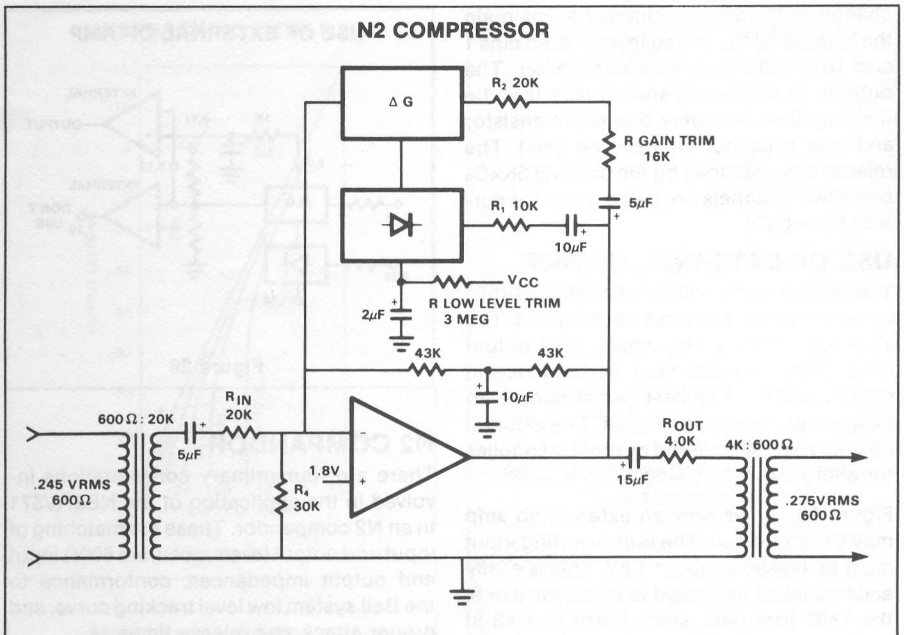


Figure 29

requires a 1.41V op amp output level. This can be provided by increasing the value of R_2 with an external resistor, which can be selected to fine trim the gain. A rearrangement of the compressor gain equation (6) allows us to determine the value for R_2.

$$R_2 = \frac{\text{Gain}^2\ R_3\ V_{in}\ \text{ave}}{R_1\ I_B} = \frac{1^2 \times 2 \times 20K \times 1.27}{10K \times 140\mu A}$$
$$= 36.3K$$

The external resistance required will thus be 36.3K - 20K = 16.3K.

The Bell compatible low level tracking characteristic is provided by the low level trim resistor from C_{rect} to V_{CC}. As shown in Figure 21 this will skew the system to a 1:1 transfer characteristic at low levels. The 2µf rectifier capacitor provides attack and release times of 3ms and 13.5ms respectively, as shown in Figures 25 and 26. The R-C-R network around the op amp provides dc feedback to bias the output at dc.

An N2 expandor is shown in Figure 30. The input level of 3.27V RMS is stepped down to 1.33V by the 600Ω: 100Ω transformer, which is terminated with a 100Ω resistor for accurate impedance matching. The output impedance is accurately set by the 150Ω output resistor and the 150Ω: 600Ω output transformer. With this configuration the 3.46V transformer output requires a 3.46V op amp output. To obtain this output level, it is necessary to increase the value of R_3 with an external trim resistor. The new value of R_3 can be found with the expandor gain equation

$$R_3 = \frac{R_1\ R_2\ I_B\ \text{Gain}}{2\ V_{in}\ \text{ave}} = \frac{10K \times 20K \times 140\mu A \times 2.6}{2 \times 1.20}$$
$$= 30.3K$$

An external addition to R_3 of 10K is required, and this value can be selected to accurately set the high level gain.

A low level trim resistor from C_{rect} to V_{CC} of about 3Meg provides matching of the Bell low level tracking curve, and the 2µf value of C_{rect} provides the proper attack and release times. A 16K resistor from the summing node to ground biases the output to $7V_{dc}$.

VOLTAGE CONTROLLED ATTENUATOR

The variable gain cell in the NE570/571 may be used as the heart of a high quality voltage controlled amplifier (VCA). Figure 31 shows a typical circuit which uses an external op amp for better performance, and an exponential converter to get a control characteristic of -6dB/V. Trim networks are shown to null out distortion and dc shift, and to fine trim gain to 0dB with zero volts of control voltage.

Op amp A_2 and transistors Q_1 and Q_2 form the exponential converter generating an exponential gain control current, which is fed into the rectifier. A reference current of 150µA, (15V and R_{20} = 100K), is attenuated a factor of two (6dB) for every volt increase in

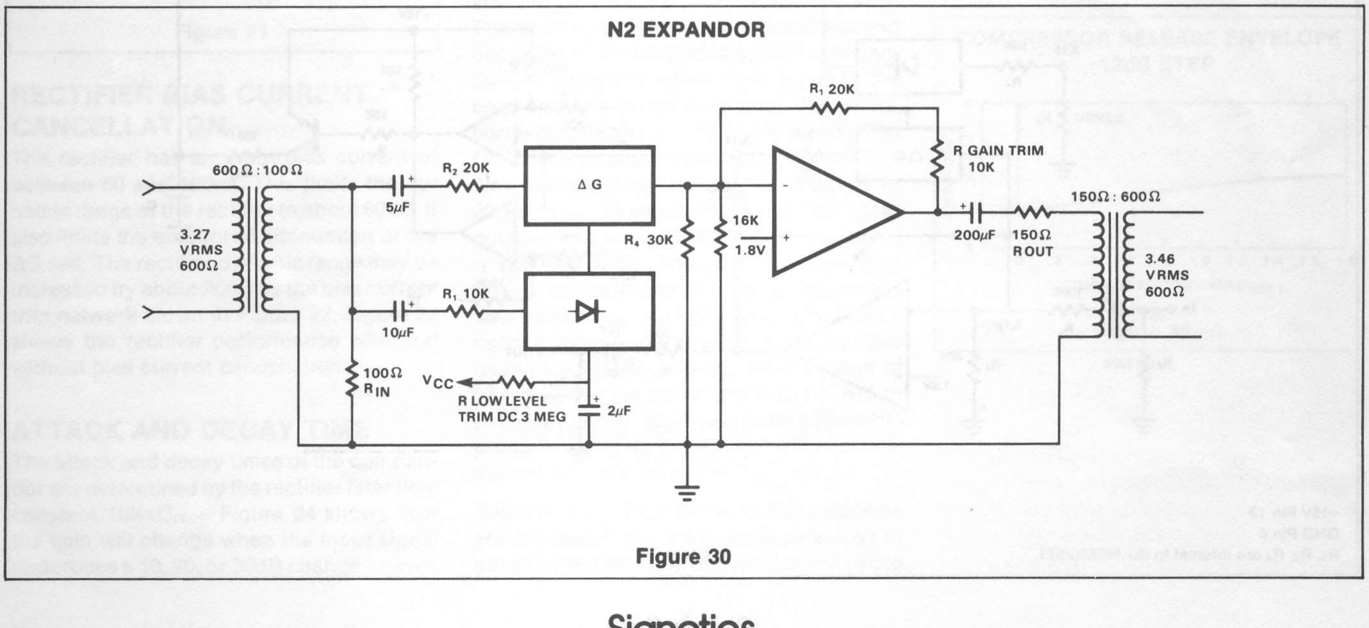


Figure 30

VOLTAGE CONTROLLED ATTENUATOR

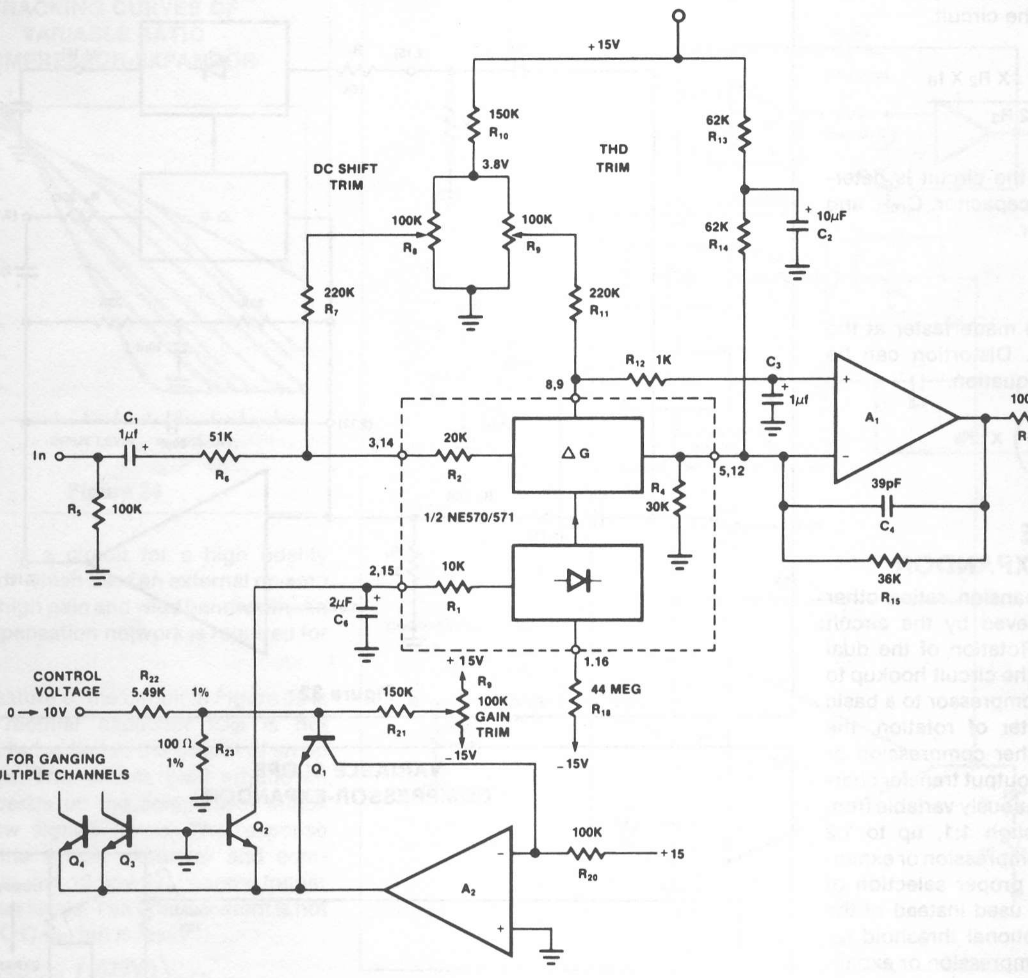


Figure 31

the control voltage. Capacitor C_6 slows down gain changes to a 20ms time constant (C_6 x R_1) so that an abrupt change in the control voltage will produce a smooth sounding gain change. R_{18} assures that for large control voltages the circuit will go to full attenuation. The rectifier bias current would normally limit the gain reduction to about 70dB. R_{18} draws excess current out of the rectifier. After approximately 50dB of attenuation at a -6dB/V slope, the slope steepens and attenuation becomes much more rapid until the circuit totally shuts off at about 9 volts of control voltage. A_1 should be a low noise high slew rate op amp. R_{13} and R_{14} establish approximately a zero volt bias at A_1's output.

With a zero volt control voltage, R_{19} should be adjusted for 0dB gain. At 1V (-6dB gain) R_9 should be adjusted for minimum distortion with a large (+10dBm) input signal. The output dc bias (A_1 output) should be measured at full attenuation (+10V control voltage) and then R_8 is adjusted to give the same value at 0dB gain. Properly adjusted, the circuit will give typically less than .1% distortion at any gain with a dc output voltage variation of only a few millivolts. The clipping level (140μA into pin 3, 14) is ±10V peak. A signal to noise ratio of 90dB can be obtained.

If several VCA's must track each other, a common exponential converter can be used. Transistors can simply be added in parallel with Q_2 to control the other channels. The transistors should be maintained at the same temperature for best tracking.

AUTOMATIC LEVEL CONTROL

The NE570 can be used to make a very high performance ALC as shown in Figure 32. This circuit hookup is very similar to the basic compressor shown in Figure 17, except that the rectifier input is tied to the input rather than the output. This makes gain inversely proportional to input level so that a 20dB drop in input level will produce a 20dB increase in gain. The output will remain fixed at a constant level. As shown, the circuit will maintain an output level of ±1dbm for an input range of +14 to -43dbm at 1khz. Additional external components will allow the output level to be adjusted. Some relevant design equations are:

$$\text{Output level} = \frac{R_1 R_2 I_B}{2 R_3}\left(\frac{V_{in}}{V_{in(avg)}}\right); \quad I_B = 140\mu A$$

$$\text{Gain} = \frac{R_1 R_2 I_B}{2 R_3 V_{in}\ (avg)} \quad \text{where}$$

$$\frac{V_{IN}}{V_{IN(avg)}} = \frac{\pi}{\sqrt{2}} = 1.11 \text{ (for sine wave)}$$

If ALC action at very low input levels is not desired, the addition of resistor R_X will limit the maximum gain of the circuit.

$$\text{Gain max.} = \frac{\frac{R_1 + R_X}{1.8V} \times R_2 \times I_B}{2 R_3}$$

The time constant of the circuit is determined by the rectifier capacitor, C_{rect}, and an internal 10K resistor.

$$\tau = 10K\ C_{rect}$$

Response time can be made faster at the expense of distortion. Distortion can be approximated by the equation.

$$\text{THD} = \left(\frac{1\mu f}{C_{rect}}\right)\left(\frac{1KHz}{freq.}\right) \times .2\%$$

VARIABLE SLOPE COMPRESSOR-EXPANDOR

Compression and expansion ratios other than 2:1 can be achieved by the circuit shown in Figure 34. Rotation of the dual potentiometer causes the circuit hookup to change from a basic compressor to a basic expandor. In the center of rotation, the circuit is 1:1, has neither compression or expansion. The (input) output transfer characteristic is thus continuously variable from 2:1 compression, through 1:1, up to 1:2 expansion. If a fixed compression or expansion ratio is desired, proper selection of fixed resistors can be used instead of the potentiometer. The optional threshold resistor will make the compression or expansion ratio deviate towards 1:1 at low levels. A wide variety of (input) output characteristics can be created with this circuit, some of which are shown in Figure 34.

HI FI COMPANDOR

The NE570 can be used to construct a high performance compandor suitable for use with music. This type of system can be used for noise reduction in tape recorders, transmission systems, bucket brigade delay lines, and digital audio systems. The circuits to be described contain features which improve performance, but are not required for all applications.

A major problem with the simple NE570 compressor (Figure 17) is the limited op amp gain at high frequencies. For weak input signals, the compressor circuit operates at high gain and the 570 op amp simply runs out of loop gain. Another problem with the 570 op amp is its limited slew rate of about .6v/μs. This is a limitation of the expandor, since the expandor is more likely to produce large output signals than a compressor.

AUTOMATIC LEVEL CONTROL

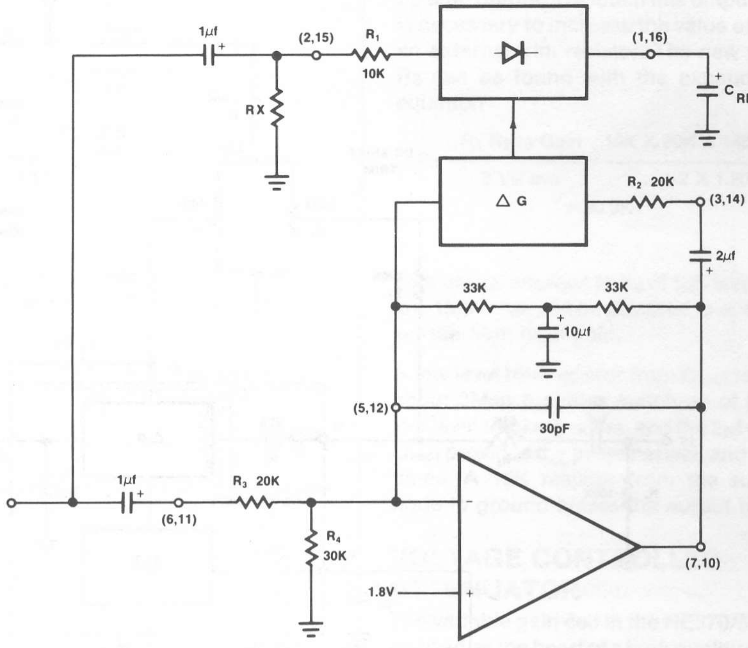


Figure 32

VARIABLE SLOPE COMPRESSOR-EXPANDOR

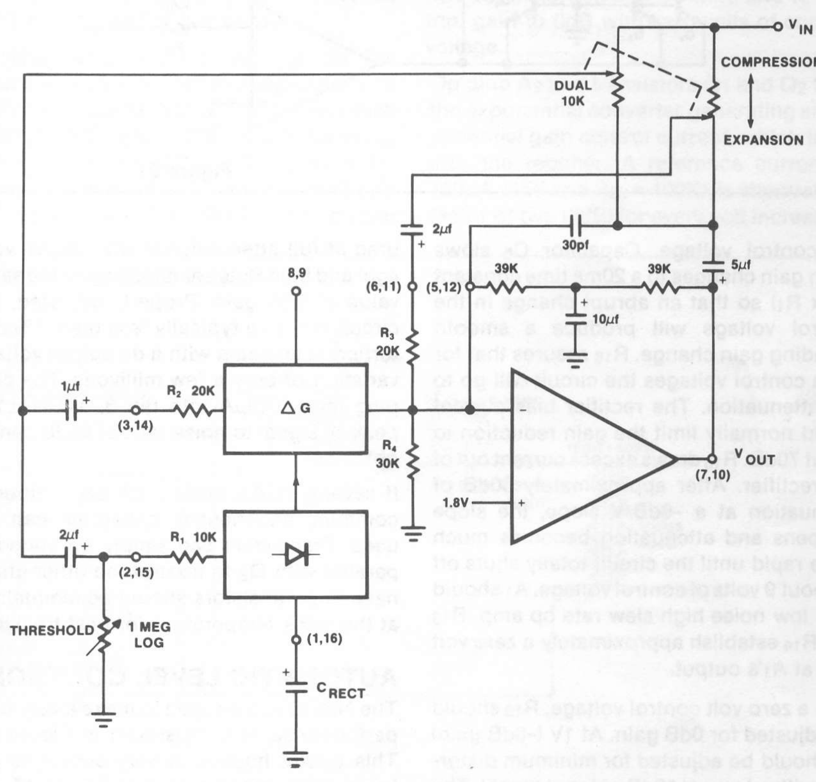


Figure 33

TYPICAL INPUT-OUTPUT TRACKING CURVES OF VARIABLE RATIO COMPRESSOR-EXPANDOR

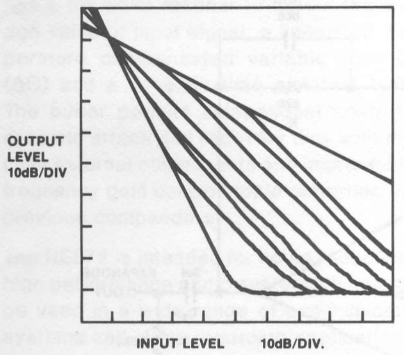


Figure 34

Figure 35 is a circuit for a high fidelity compressor which uses an external op amp and has a high gain and wide bandwidth. An input compensation network is required for stability.

Another feature of the circuit in Figure 35 is that the rectifier capacitor (C_9) is not grounded, but is tied to the output of an op amp circuit. This circuit, built around an LM324, speeds up the compressor attack time at low signals levels. The response times of the simple expandor and compressor (Figures 16 and 17) become longer at low signal levels. The time constant is not simply $10K \times C_{rect}$, but is really

$$\left(10K + 2\left(\frac{.026V}{I_{rect}}\right)\right) \times C_{rect}.$$

When the rectifier input level drops from 0dBm to -30dBm, the time constant increases from $10.7K \times C_{rect}$ to $32.6K \times C_{rect}$. In systems where there is unity gain between the compressor and expandor, this will cause no overall error. Gain or loss between the compressor and expandor will be a mistracking of low signal dynamics. The circuit with the LM324 will greatly reduce this problem for systems which cannot guarantee the unity gain.

When a compressor is operating at high gain, (small input signal), and is suddenly hit with a signal, it will overload until it can reduce its gain. Overloaded the output will attempt to swing rail to rail. This compressor is limited to approximately a 7V peak to peak output swing by the brute force clamp diodes D_3 and D_4. The diodes cannot be placed in the feedback loop because their capacitance would limit high frequency gain. The purpose of limiting the output swing is to avoid overloading any succeeding circuit such as a tape recorder input.

HI-FI COMPRESSOR WITH PRE-EMPHASIS

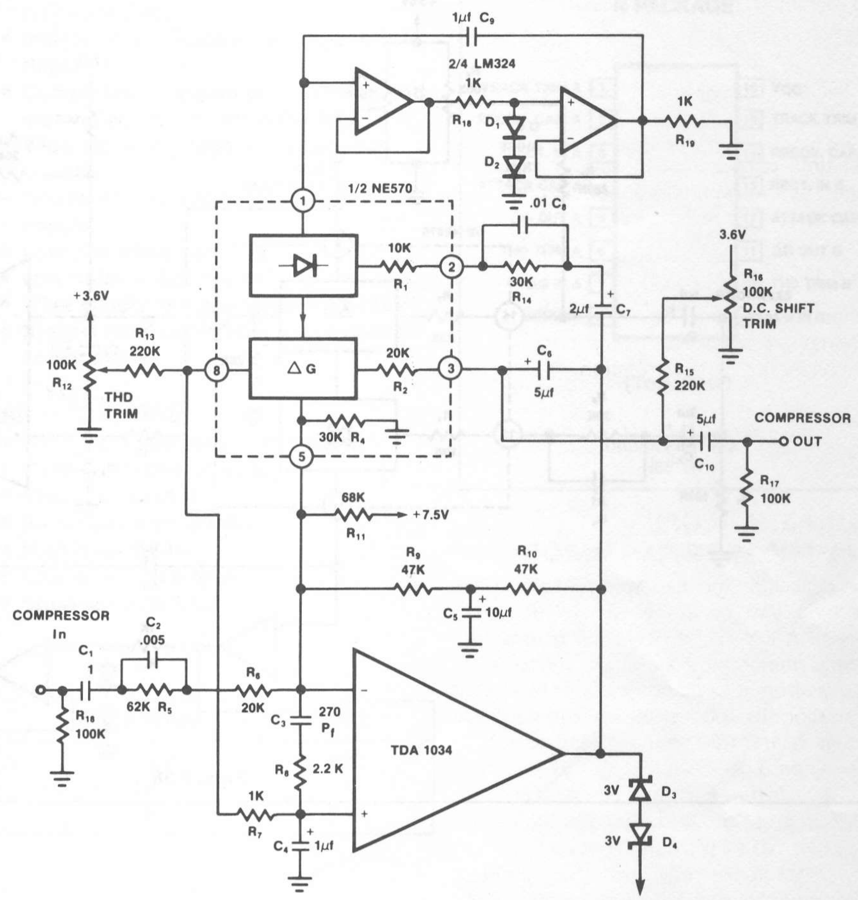


Figure 35

The time it takes for the compressor to recover from overload is determined by the rectifier capacitor C_9. A smaller capacitor will allow faster response to transients, but will produce more low frequency third harmonic distortion due to gain modulation. A value of 1µf seems to be a good compromise value and yields good subjective results. Of course, the expandor should have exactly the same value rectifier capacitor for proper transient response. Systems which have good low frequency amplitude and phase response can use compandors with smaller rectifier capacitors, since the third harmonic distortion which is generated by the compressor will be undistorted by the expandor.

Simple compandor systems are subject to a problem known as breathing. As the system is changing gain, the change in the background noise level can sometimes be heard. The compressor in Figure 35 contains a high frequency pre-emphasis circuit (C_2, R_5 and C_8, R_{14}), which helps solve this problem. Matching de-emphasis on the expandor is required. More complex designs could make the pre-emphasis variable and further reduce breathing.

The expandor to complement the compressor is shown in Figure 36. Here an external op amp is used for high slew rate. Both the compressor and expandor have unity gain levels of 0dBm. Trim networks are shown for distortion (THD) and dc shift. The distortion trim should be done first, with an input of 0dBm at 10kHz. The dc shift should be adjusted for minimum envelope bounce with tone bursts. When applied to consumer tape recorders, the subjective performance of this system is excellent.

CIRCUIT DESCRIPTION AND APPLICATIONS NE570/571/SA571

HI-FI EXPANDOR WITH DE-EMPHASIS

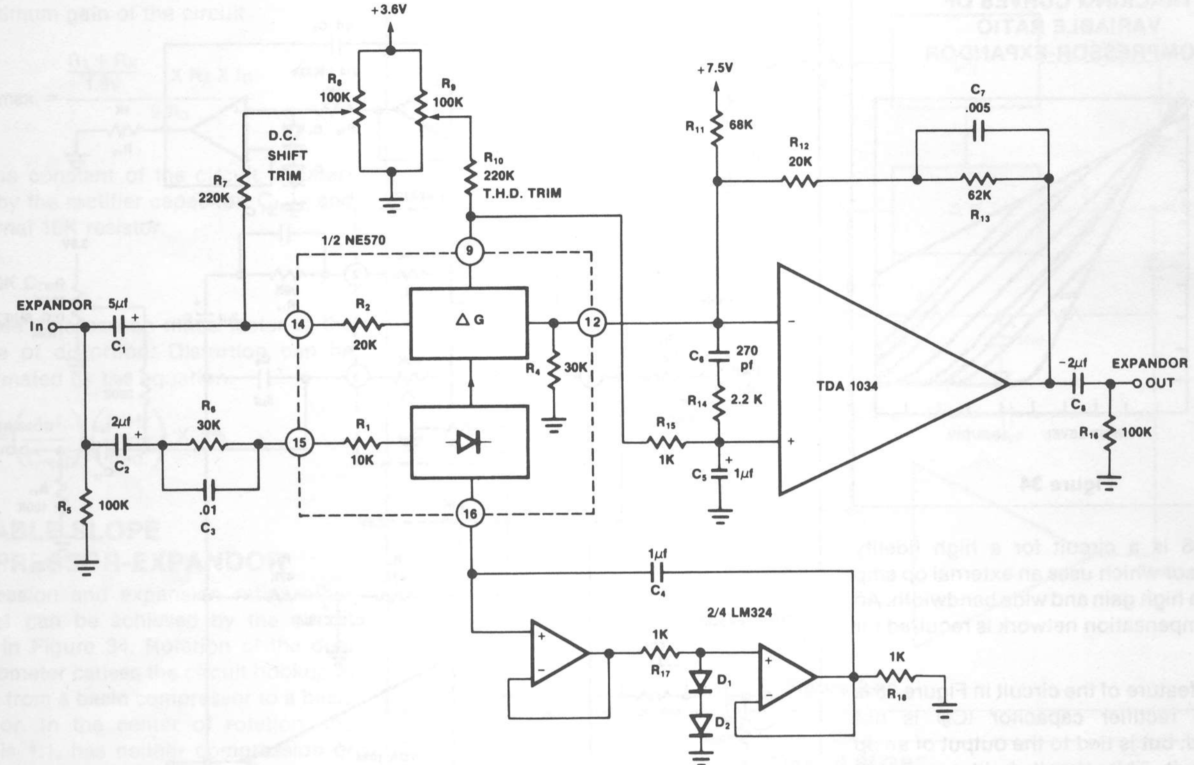


Figure 36

PROGRAMMABLE ANALOG COMPANDOR NE572

DESCRIPTION

The NE572 is a dual channel, high performance gain control circuit in which either channel may be used for dynamic range compression or expansion. Each channel has a full wave rectifier to detect the average value of input signal; a linearized, temperature compensated variable gain cell (ΔG) and a dynamic time constant buffer. The buffer permits independent control of dynamic attack and recovery time with minimum external components and improved low frequency gain control ripple distortion over previous compandors.

The NE572 is intended for noise reduction in high performance audio systems. It can also be used in a wide range of communication systems and video recording applications.

FEATURES

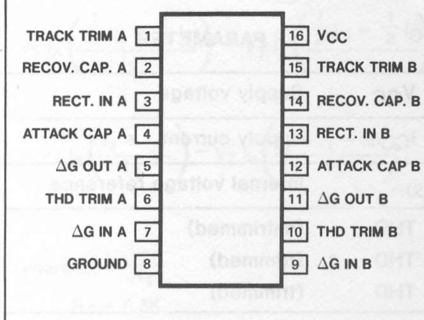
- Independent control of attack and recovery time.
- Improved low frequency gain control ripple
- Complementary gain compression and expansion with external Op Amp
- Wide dynamic range—greater than 110dB
- Temperature compensated gain control
- Low distortion gain cell
- Low noise—6μV typical
- Wide supply voltage range—6V-22V
- System level adjustable with external components.

APPLICATIONS

- Dynamic noise reduction system
- Voltage control amplifier
- Stereo expandor
- Automatic level control
- High level limiter
- Low level noise gate
- State variable filter

PIN CONFIGURATION

N PACKAGE



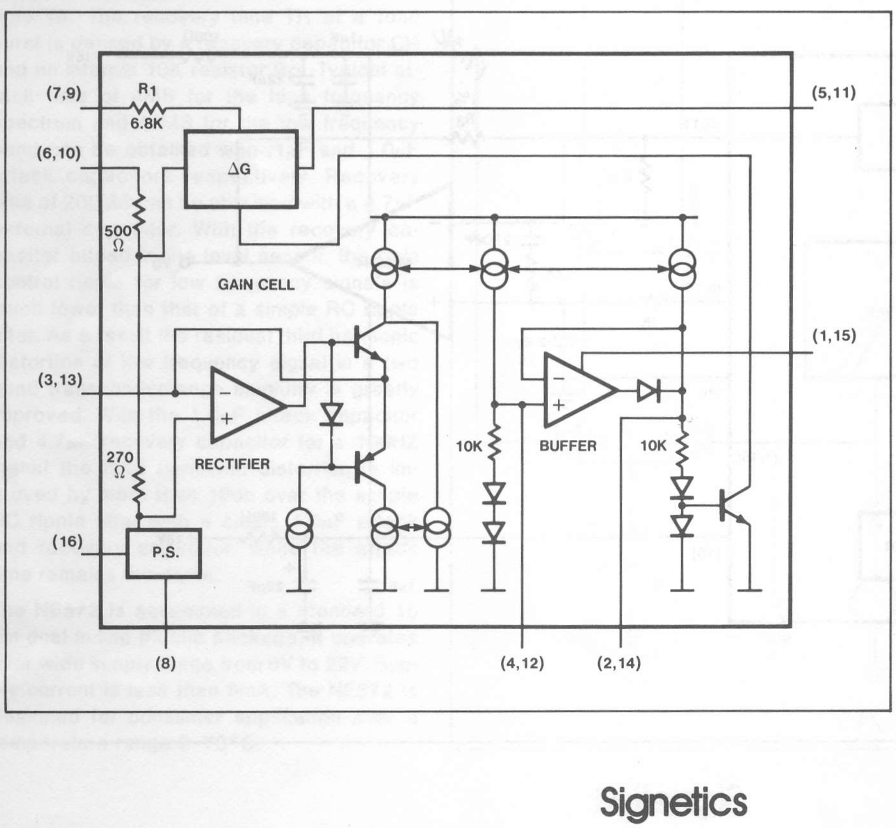
(Top view)

ORDER PART NO.
NE572N

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	22	VDC
T_A	Operating temperature range	0 to 70	°C
P_D	Power dissipation	500	mW

BLOCK DIAGRAM



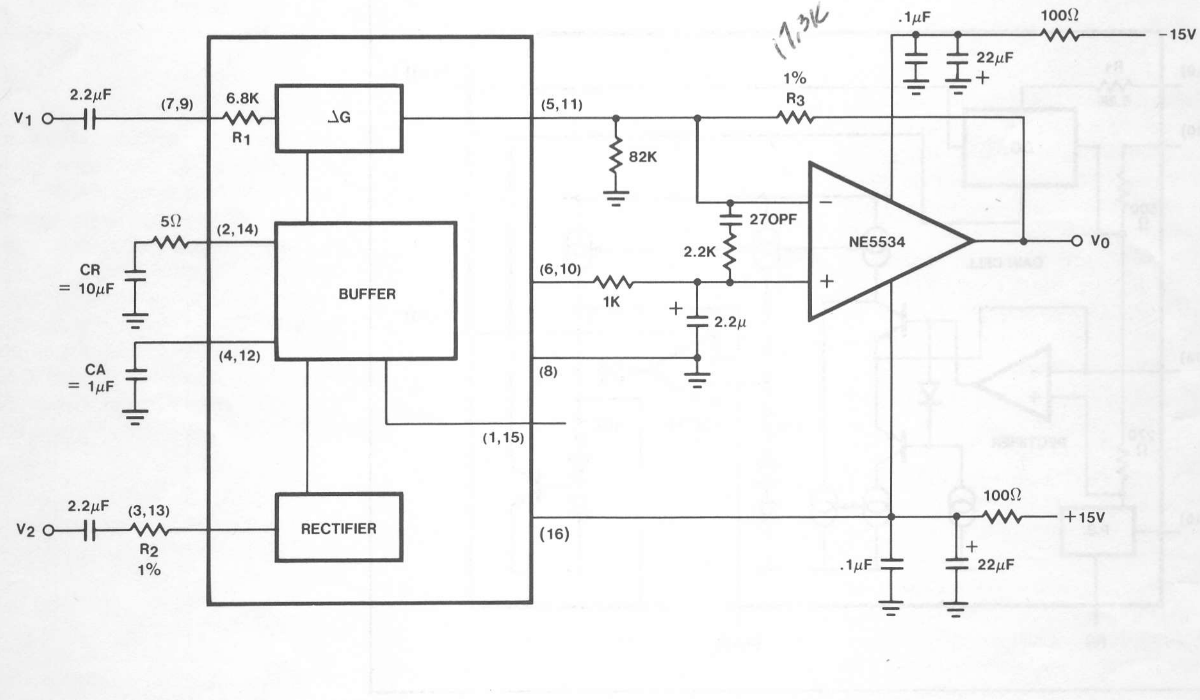
PROGRAMMABLE ANALOG COMPANDOR NE572

ELECTRICAL CHARACTERISTICS

Standard Test Conditions (unless otherwise noted) V_{CC} = 15V TA = 25°C Expandor mode (see test circuit) Input signals at unity gain level = 100mV RMS at 1KHz, $V_1 = V_2$, R_2 = 3.3K R_3 = 17.3K

	PARAMETER	TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
V_{CC}	Supply voltage		6		22	V_{DC}
I_{CC}	Supply current	No Signal			6	mA
	Internal voltage reference		2.3	2.5	2.7	V_{DC}
THD	(untrimmed)	1kHz $C_A = 1.0\mu F$		.2	1.0	%
THD	(trimmed)	1kHz $C_R = 10\mu F$		.05		%
THD	(trimmed)	100Hz		.25		%
	No signal output noise	Input to V_1 and V_2 grounded (20-20kHz)		6	25	uV
	DC level shift (untrimmed)	Input change from no signal to 100mV RMS		±20	±50	MV
	Unity gain level		−1	0	+1	dB
	Large signal distortion	$V_1 = V_2$ = 400mV		0.7	3.0	%
	Tracking error measured relative to value at unity gain output	Rectifier input V_2 = +6dB		±.2		dB
		−30dB		±.5	−1.5 +.8	
	Channel crosstalk	200mV RMS into channel A, measured output on channel B	60			dB
	Power supply rejection ratio	120Hz		70		dB

TEST CIRCUIT



AUDIO SIGNAL PROCESSING IC COMBINES VCA AND FAST ATTACK-SLOW RECOVERY LEVEL SENSOR

In high performance audio gain control applications it is desirable to independently control the attack and recovery time of the gain control signal. This is true, for example, in compandor applications for noise reduction. In high end systems the input signal is usually split into two or more frequency bands to optimize the dynamic behavior for each band. This reduces low frequency distortion due to control signal ripple, phase distortion, high frequency channel overload and noise modulation. Because of the expense in hardware, multiple band signal processing up to now was limited to professional audio applications.

With the introduction of the Signetics NE572 this high performance noise reduction concept becomes feasible for consumer hi fi applications. The NE572 is a dual channel gain control IC. Each channel has a linearized, temperature compensated gain cell and an improved level sensor. In conjunction with an external low noise op amp for current to voltage conversion, the VCA features low distortion, low noise and wide dynamic range. The novel level sensor which provides gain control current for the VCA gives lower gain control ripple and independent control of fast attack, slow recovery dynamic response. An attack capacitor CA with an internal 10K resistor RA defines the attack time TA. The recovery time TR of a tone burst is defined by a recovery capacitor CR and an internal 10K resistor R_R. Typical attack time of 4MS for the high frequency spectrum and 40MS for the low frequency band can be obtained with .1μF and 1.0μF attack capacitors respectively. Recovery time of 200MS can be obtained with a 4.7μF external capacitor. With the recovery capacitor added in the level sensor, the gain control ripple for low frequency signals is much lower than that of a simple RC ripple filter. As a result the residual third harmonic distortion of low frequency signal in a two quad transconductance amplifier is greatly improved. With the 1.0μF attack capacitor and 4.7μF recovery capacitor for a 100HZ signal the third harmonic distortion is improved by more than 10db over the simple RC ripple filter with a single 1.0μF attack and recovery capacitor, while the attack time remains the same.

The NE572 is assembled in a standard 16 pin dual in line plastic package. It operates over wide supply range from 6V to 22V. Supply current is less than 6mA. The NE572 is designed for consumer application over a temperature range 0-70°C.

NE572 BASIC APPLICATIONS

Description

The NE572 consists of two linearized, temperature compensated gain cells (ΔG) each with a full-wave rectifier and a buffer amplifier as shown in the block diagram. The two channels share a 2.5V common bias reference derived from the power supply but otherwise operate independently. Because of inherent low distortion, low noise and the capability to linearize large signals, a wide dynamic range can be obtained. The buffer amplifiers are provided to permit control of attack time and recovery time independent of each other. Partitioned as shown in the block diagram, the IC allows flexibility in the design of system levels that optimize DC shift, ripple distortion, tracking accuracy and noise floor for a wide range of application requirements.

Gain Cell

Figure 1 shows the circuit configuration of the gain cell. Bases of the differential pairs $Q_1 - Q_2$ and $Q_3 - Q_4$ are both tied to the output and inputs of OPA A_1. The negative feedback through Q_1 holds the V_{BE} of $Q_1 - Q_2$ and the V_{BE} of $Q_3 - Q_4$ equal. The following relationship can be derived from the transistor model equation in the forward active region.

$$\Delta V_{BE_{Q_3-Q_4}} = \Delta V_{BE_{Q_1-Q_2}} \qquad -(1)$$

$$(V_{BE} = V_T\, l_n\, IC/IS)$$

$$V_T\, l_n\left(\frac{\frac{1}{2}I_G + \frac{1}{2}I_O}{I_S}\right) - V_T\, l_n\left(\frac{\frac{1}{2}I_G - \frac{1}{2}I_O}{I_S}\right)$$

$$= V_T\, l_n\left(\frac{I_1 + I_{in}}{I_S}\right) - V_T\, l_n\left(\frac{I_2 - I_1 - I_{in}}{I_S}\right) \qquad -(2)$$

where $I_{in} = \frac{V_{in}}{R_1}$

$R_1 = 6.8K$
$I_1 = 140\mu A$
$I_2 = 280\mu A$

I_O is the differential output current of the gain cell and I_G is the gain control current of the gain cell.

If all transistors Q_1 through Q_4 are of the same size, equation (2) can be simplfied to:

$$I_O = \frac{2}{I_2} \cdot I_{in} \cdot I_G - \frac{1}{2}(I_2 - 2I_1) \cdot I_G \qquad -(3)$$

The first term of eqn. (3) shows the multiplier relationship of a linearized two quadrant transconductance amplifier. The second term is the gain control feed through due to the mismatch of devices. In the design this

BASIC GAIN CELL SCHEMATIC

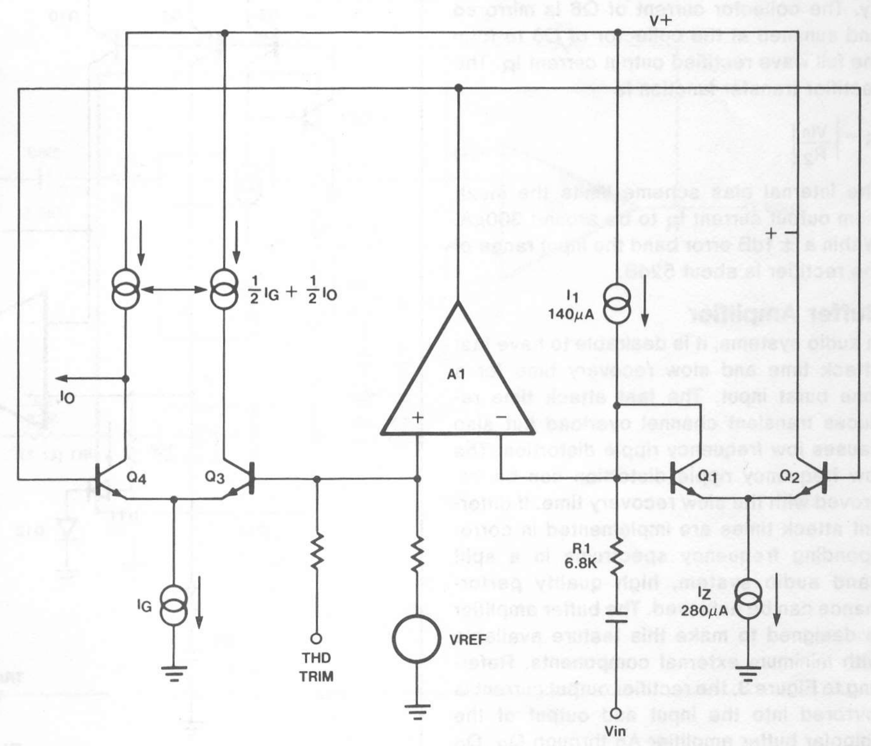


Figure 1

has been minimized by large matched devices and careful layout. Offset voltage is caused by the device mismatch and it leads to even harmonic distortion. The offset voltage can be trimmed out by feeding a current source within $\pm 25\mu A$ into the THD trim pin. The residual distortion is third harmonic distortion and is caused by gain control ripple. In a compandor system, available control of fast attack and slow recovery improves ripple distortion significantly. At the unity gain level of 100mV, the gain cell gives THD (total harmonic distortion) of .17% TYP. Output noise with no input signals is only $6\mu V$ in the audio spectrum (10HZ-20KHZ). The output current I_O must feed the virtual ground input of an operational amplifier with a resistor from output to inverting input. The non-inverting input of the operational amplifier has to be biased at VREF if the output current I_O is dc coupled.

Rectifier

The rectifier is a full-wave design as shown in Figure 2. The input voltage is converted to current through the input resistor R2 and turns on either Q5 or Q6 depending on the signal polarity. Deadband of the voltage to current converter is reduced by the loop gain of the gain block A2. If AC coupling is used, the rectifier error comes only from input bias current of gain block A2. The input bias current is typically about 70nA. Frequency response of the gain block A2 also causes second order error at high frequency. The collector current of Q6 is mirrored and summed at the collector of Q5 to form the full wave rectified output current I_R. The rectifier transfer function is

$$I_R = \left| \frac{V_{in}}{R_2} \right| \qquad -(4)$$

The internal bias scheme limits the maximum output current I_R to be around $300\mu A$. Within a $\pm$ 1dB error band the input range of the rectifier is about 52dB.

Buffer Amplifier

In audio systems, it is desirable to have fast attack time and slow recovery time for a tone burst input. The fast attack time reduces transient channel overload but also causes low frequency ripple distortion. The low frequency ripple distortion can be improved with the slow recovery time. If different attack times are implemented in corresponding frequency spectrums in a split band audio system, high quality performance can be achieved. The buffer amplifier is designed to make this feature available with minimum external components. Referring to Figure 3, the rectifier output current is mirrored into the input and output of the unipolar buffer amplifier A_3 through Q_8, Q_9 and Q_{10}. Diodes D_{11} and D_{12} improve

SIMPLIFIED RECTIFIER SCHEMATIC

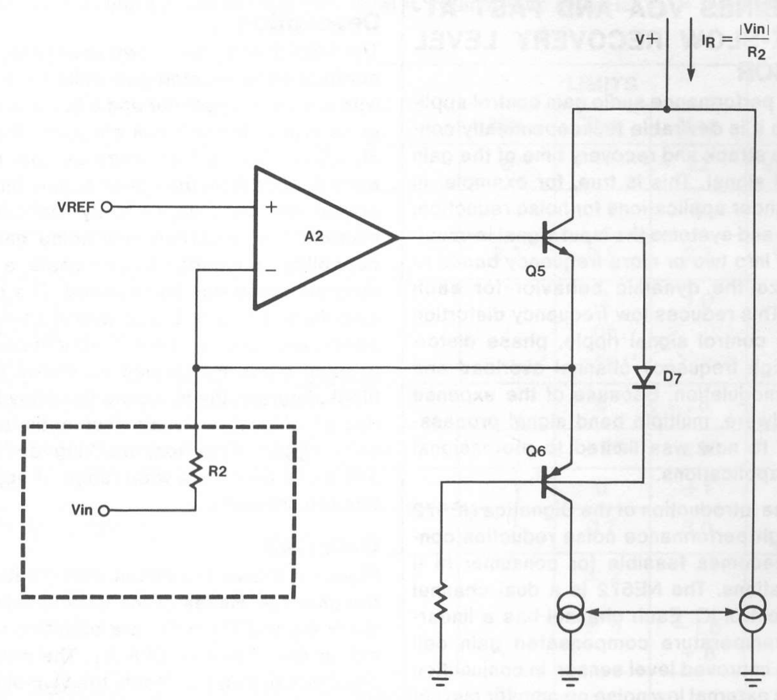


Figure 2

BUFFER AMPLIFIER SCHEMATIC

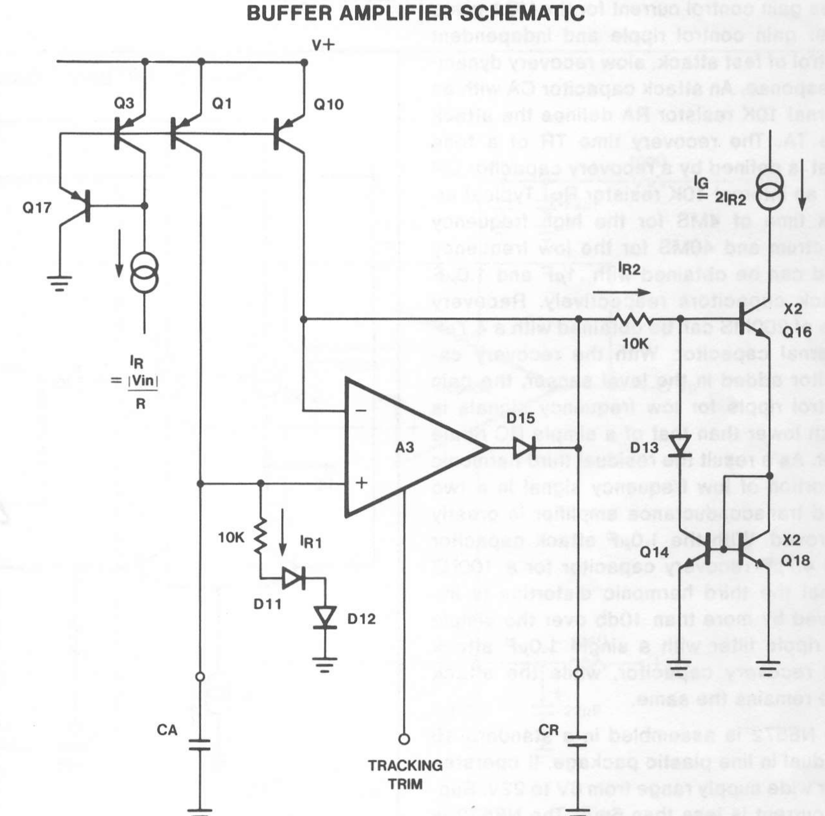


Figure 3

tracking accuracy and provide common mode bias for A_3. For a positive going input signal, the buffer amplifier acts like a voltage follower. Therefore, the output impedance of A_3 makes the contribution of capacitor CR to attack time insignificant. Neglecting diode impedance the gain Ga(t) for ΔG can be expressed as follows.

$$Ga(t) = (Ga_{INT} - Ga_{FNL})\, e^{\frac{-t}{\tau A}} + Ga_{FNL}$$

Gint = Initial Gain

$\tau A = R_A \cdot CA = 10K \cdot CA$ Gfnl = Final Gain

where τA is the attack time constant and RA is a 10K internal resistor. Diode D_{15} opens the feedback loop of A_3 for a negative going signal if the value of capacitor CR is larger than capacitor CA. The recovery time depends only on CR • R_R. If the diode impedance is assumed negligible, the dynamic gain G_R (t) for ΔG is expressed as follows.

$$G_R(t) = (G_{R\,INT} - G_{R\,FNL})\, e^{\frac{-t}{\tau R}} + G_{R\,FNL}$$

$\tau R = R_R \cdot CR = 10K \cdot CR$

where τR is the recovery time constant and R_R is a 10K internal resistor. The gain control current is mirrored to the gain cell through Q_{14}. The low level gain errors due to input bias current of A_2 and A_3 can be trimmed through the tracking trim PIN into A_3 with a current source of ±3μA.

Basic Expandor

Figure 4 shows an application of the circuit as a simple expandor. The gain expression of the system is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{2}{I_1} \cdot \frac{R_3 \cdot V_{IN\,(AVG)}}{R_2 \cdot R_1} \qquad -(1)$$

Both the resistors R_1 and R_2 are tied to internal summing nodes. R_1 is a 6.8K internal resistor. The maximum input current into the gain cell can be as large as 140μA. This corresponds to a voltage level of 140μA • 6.8K = 952mV peak. The input peak current into the rectifier is limited to 300μA by the internal bias system. Note that the value of R_1 can be increased to accommodate higher input level. R_2 and R_3 are external resistors. It is easy to adjust the ratio of R3/R2 for desirable system voltage and current levels. A small R2 results in higher gain control current and smaller static and dynamic tracking error. However, an impedance buffer A_1 may be necessary if the input is voltage drive with large source impedance.

The gain cell output current feeds the summing node of the external OPA A_2. R_3 and A_2 convert the gain cell output current to the output voltage. In high performance applications, A_2 has to be low noise, high speed and wide band so that the high performance output of the gain cell will not be degraded. The non-inverting input of A_2 can be biased at the low noise internal reference PIN 6 or 10. Resistor R_4 is used to biased up the output DC level of A_2 for maximum swing. The output DC level of A_2 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_3}{R_4}\right) - V_B \frac{R_3}{R_4} \qquad -(2)$$

V_B can be tied to a regulated power supply for a dual supply system and be grounded for a single supply system. CA sets the attack time constant and CR sets the recovery time constant.

BASIC EXPANDOR SCHEMATIC

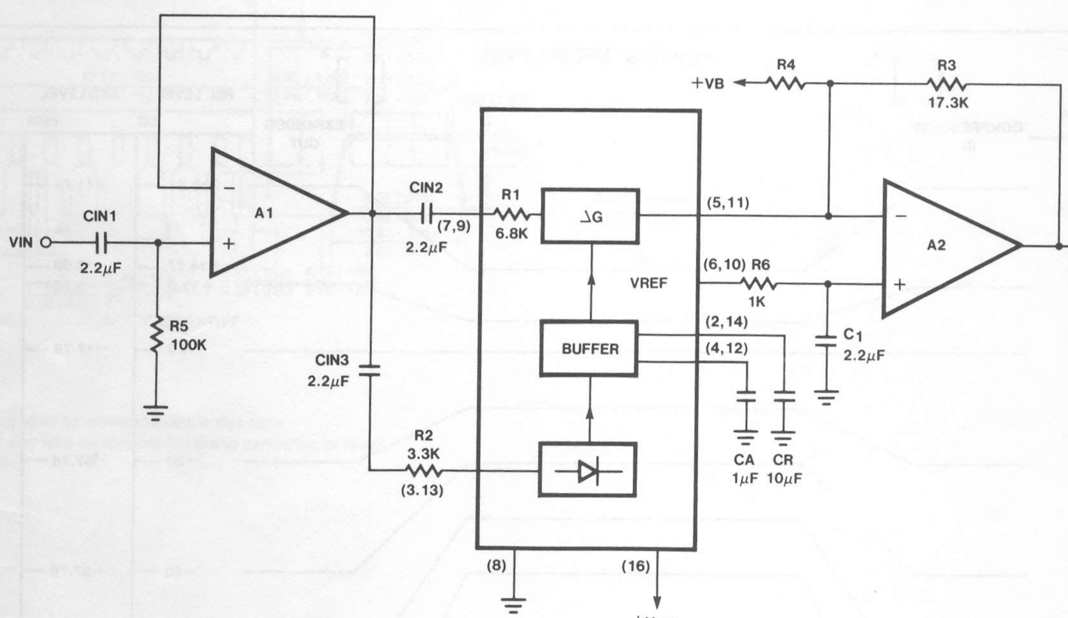


Figure 4

CIRCUIT DESCRIPTION AND APPLICATIONS NE572

Basic Compressor

Figure 5 shows the hook-up of the circuit as a compressor. The IC is put in the feedback loop of the OPA A_1. The system gain expression is as follows:

$$\frac{V_{OUT}}{V_{IN}} = \frac{I_1}{2} \cdot \frac{R_2 \cdot R_1}{R_3 \cdot V_O\,(AVG)} \qquad -(1)$$

RDC1, RDC2, and CDC form a dc feedback for A_1. The output DC level of A_1 is given by

$$V_{ODC} = V_{REF}\left(1 + \frac{R_{DC1} + R_{DC2}}{R_4}\right) - V_B \cdot \left(\frac{R_{DC1} + R_{DC2}}{R_4}\right) \qquad -(2)$$

The zener diodes D_1 and D_2 are used for channel overload protection.

Basic Compandor System

The above basic compressor and expandor can be applied to systems such as tape/disc noise reduction, digital audio, bucket brigade delay lines. Additional system design techniques such as bandlimiting, band splitting, pre-emphasis, de-emphasis and equalization are easy to incorporate. The IC is a versatile functional block to achieve a high performance audio system. Figure 6 shows the system level diagram for reference.

BASIC COMPRESSOR SCHEMATIC

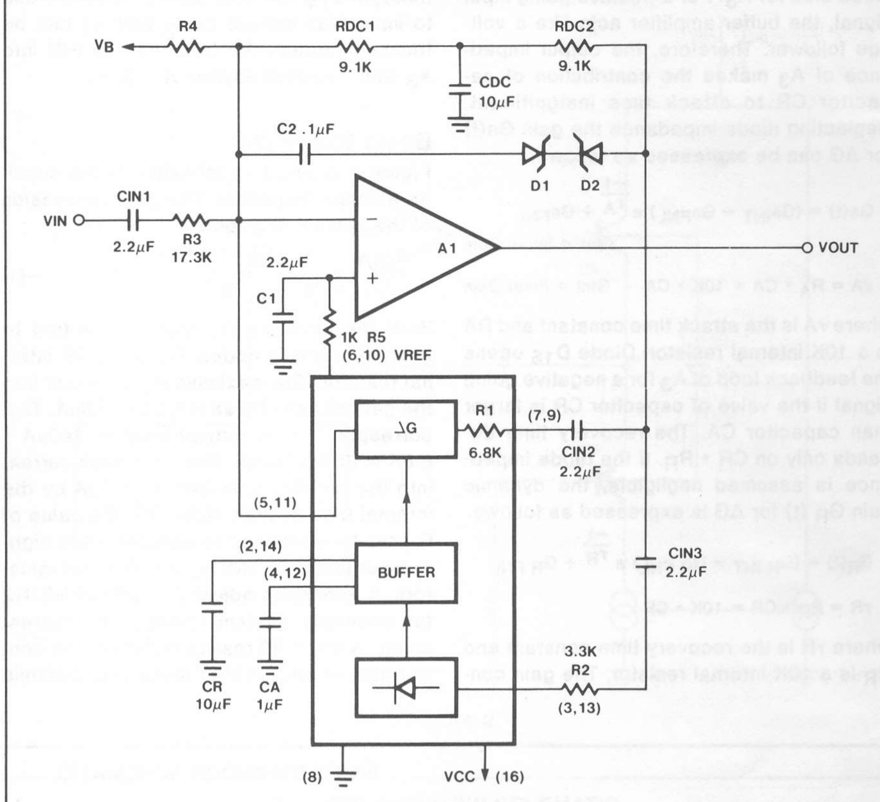


Figure 5

NE572 SYSTEM LEVEL

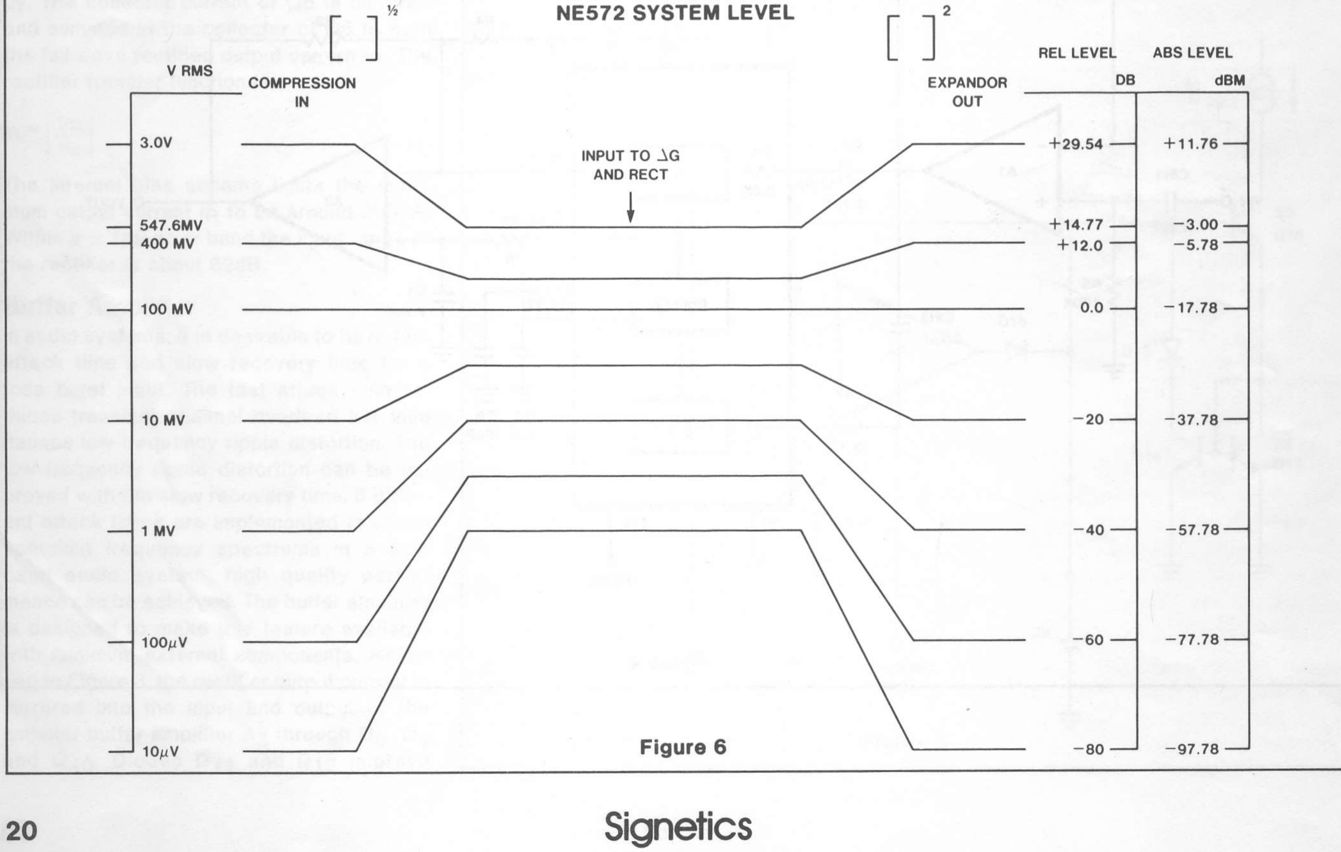


Figure 6